

Model Name: B560 AORUS PRO AX

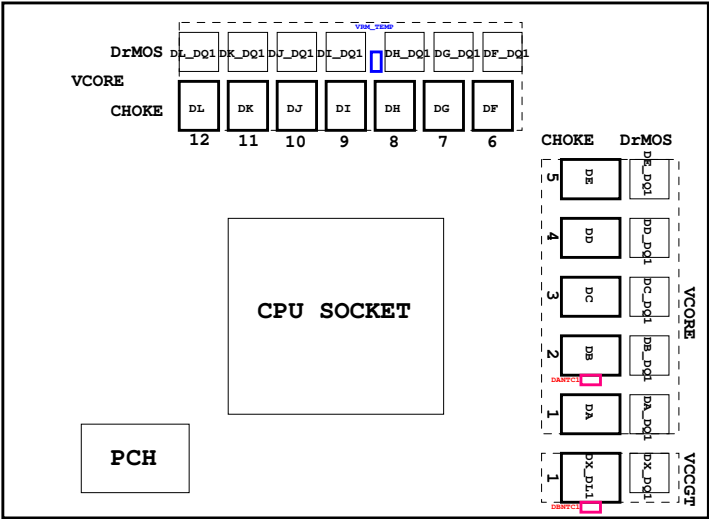
SHEET

TITLE

rev 1.0

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1200-A (RKL_R0.1)
05	CPU_LGA1200-B-DDR4 (RKL_R0.1)
06	CPU_LGA1200-C (RKL_R0.1)
07	CPU_LGA1200-D (RKL_R0.1)
08	DDR 4 CHANNEL A (CML_R0.1)
09	DDR 4 CHANNEL B (CML_R0.1)
10	PCH CLK,DMI,CNVI (RKL_R0.1)
11	PCH SPI,USB (RKL_R0.1)
12	PCH PCIE,SATA (RKL_R0.1)
13	PCH ESPI,MISC (RKL_R0.1)
14	PCH GPP,HDA (RKL_R0.1)
15	PCH PWR, GND (RKL_R0.1)
16	Heatsink
17	ITE ITE8689 (RKL_R0.1)
18	HWM (RKL_R0.1)
19	FAN CTRL-CFL-SIO_5 FAN (RKL_R0.1)
20	Single BIOS for CS mode (RKL_R0.1)
21	PCI EXPRESS X16 SLOT (REV0.3)
22	PCI EXPRESS X4 SLOT (PCH) (REV0.51)
23	PCI EXPRESS X1 *3 (REV0.51)
24	SATA
25	M.2 x4 (A) (RKL_R0.1)
26	(RKL_R0.1)
27	(RKL_R0.1)
28	M.2 x4 (P) (RKL_R0.1)
29	COM,LPT,TPM, THB (CML_R0.94)
30	ISL69269_L=0.15u (RKL_R0.1)
31	RAA229001_L=0.15u (RKL_R0.1)
32	VCORE_PSTAGE-1_L=0.15u (RKL_R0.1)
33	VCORE_PSTAGE-2_L=0.15u (RKL_R0.1)
34	VCORE_PSTAGE-3_L=0.15u (RKL_R0.1)
35	VCCGT_PSTAGE_L=0.15u (RKL_R0.1)
36	VCCSA_MOS (RKL_R0.1)
37	VCCIO-Ferrite-Z系列 (RKL_R0.1)
38	VCCIO2-Ferrite-Z系列 (RKL_R0.1)
39	RT8120_DDR_CHOKE-Ferrite-2L (RKL_R0.1)
40	RT8120_VPP_CHOKE-合金
41	NCP81269_VCC18_PCH
42	RT8068_VCC1V8_PRIM
43	DISCRETE POWER (REV0.1)
44	ATX POWER , A_-PROCHOT
45	HDMI_NO LS (CML_R0.94)
46	CNVi_M2_WIFI (CML_R0.94)
47	Redriver_RTS5461_A (RKL_R0.1)
48	RTS5441E_A_Type-C (RKL_R0.1)
49	Redriver_RTS5461_B (RKL_R0.1)

SHEET	TITLE
50	R_USB30x4 (CML_R0.94)
51	GENESYS GL850S_1 (RKL_R0.1)
52	GENESYS GL850S_2 (RKL_R0.1)
53	F_USB20 (CML_R0.94)
54	F_U32 (CML_R0.94)
55	KB_MS_USB (CML_R0.94)
56	RTS5441E_B_Front1 (RKL_R0.1)
57	INTEL I219 (CML_R0.3)
58	U32_LAN CONNECTOR-I219 (CML_R0.3)
59	Realtek ALC1200 (RKL_R0.6)
60	REAR AUDIO JACK (RKL_R0.6)
61	CPU POWER-1 (RKL_R0.1)
62	CPU POWER-1 (RKL_R0.1)
63	NCT3933
64	F_PANEL
65	IT5702 (RKL_R1.0)
66	PCH/AUDIO/DEBUG/C_LED1/2 (RKL_R1.0)
67	D_LED1/D_LED2
68	SMBUS SWITCH (RKL_R0.1)
69	CKG (RKL_R0.1)
70	EMI-ESD
71	POWER MAP
72	NTC MAP



rev1.0

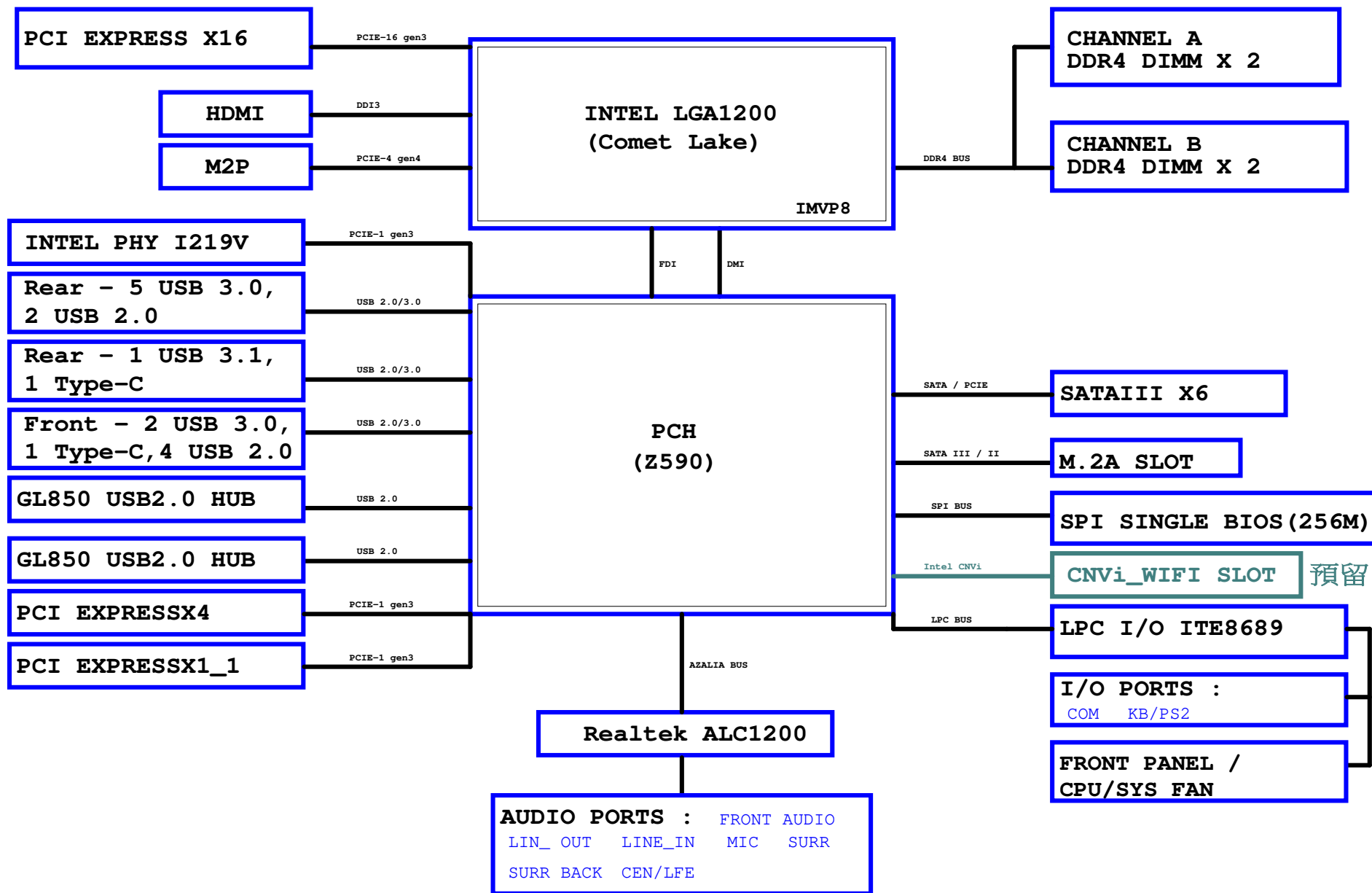
Circuit or PCB layout change

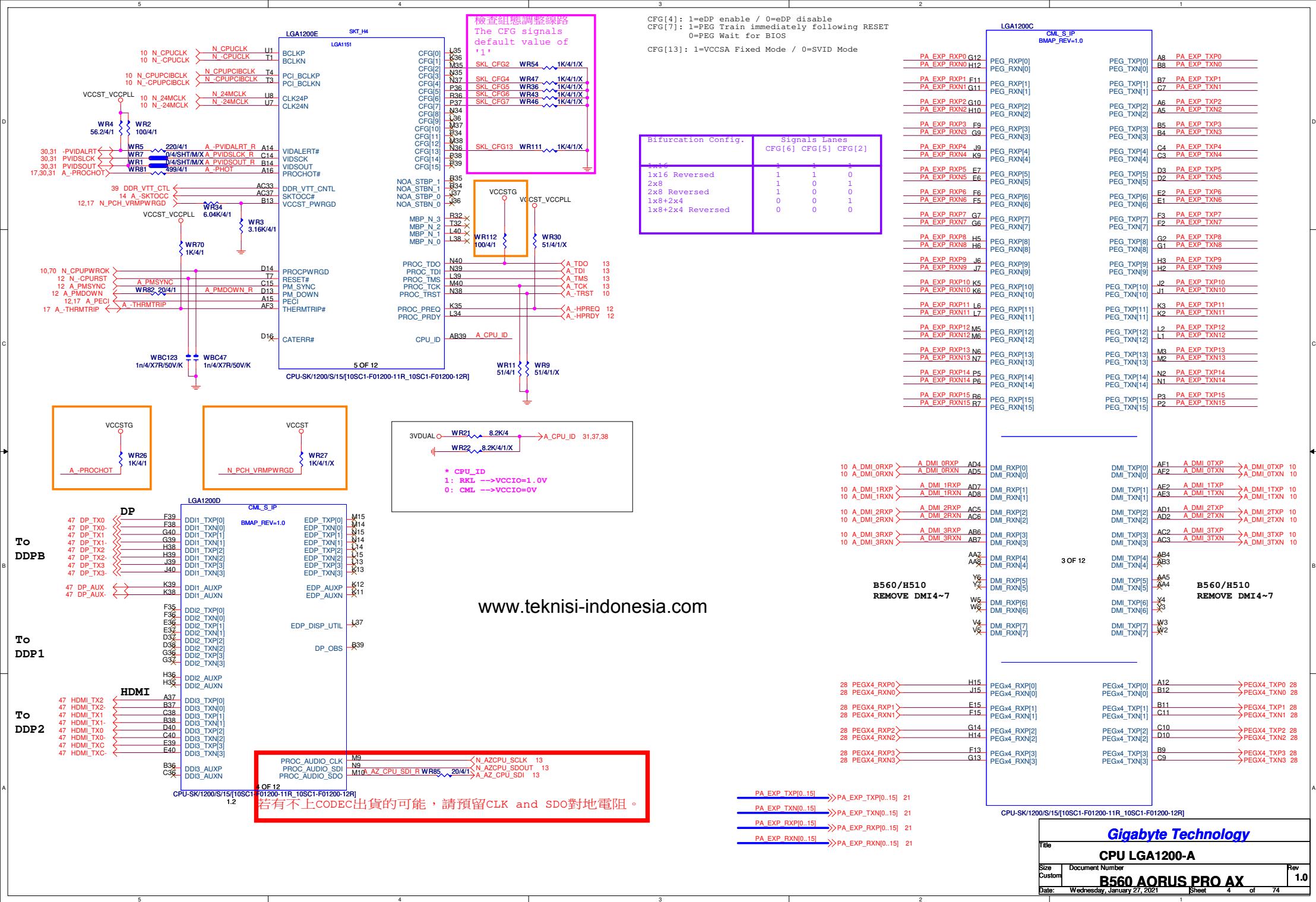
Component value change history

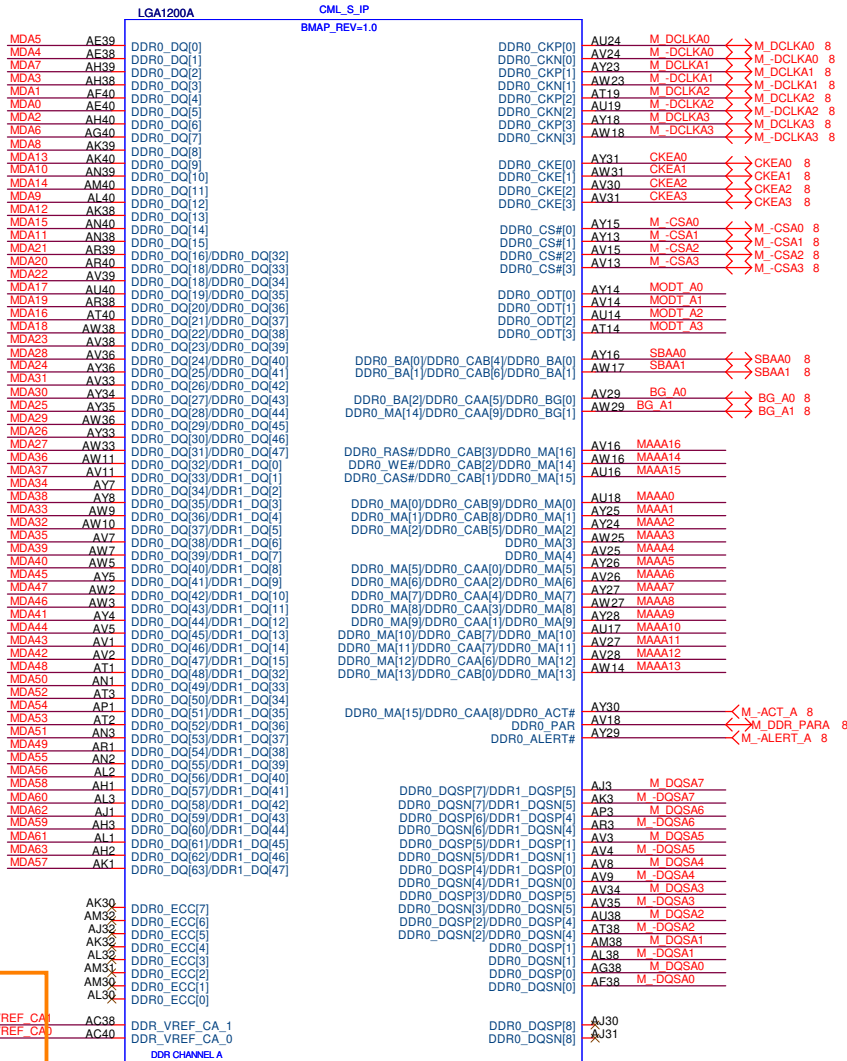
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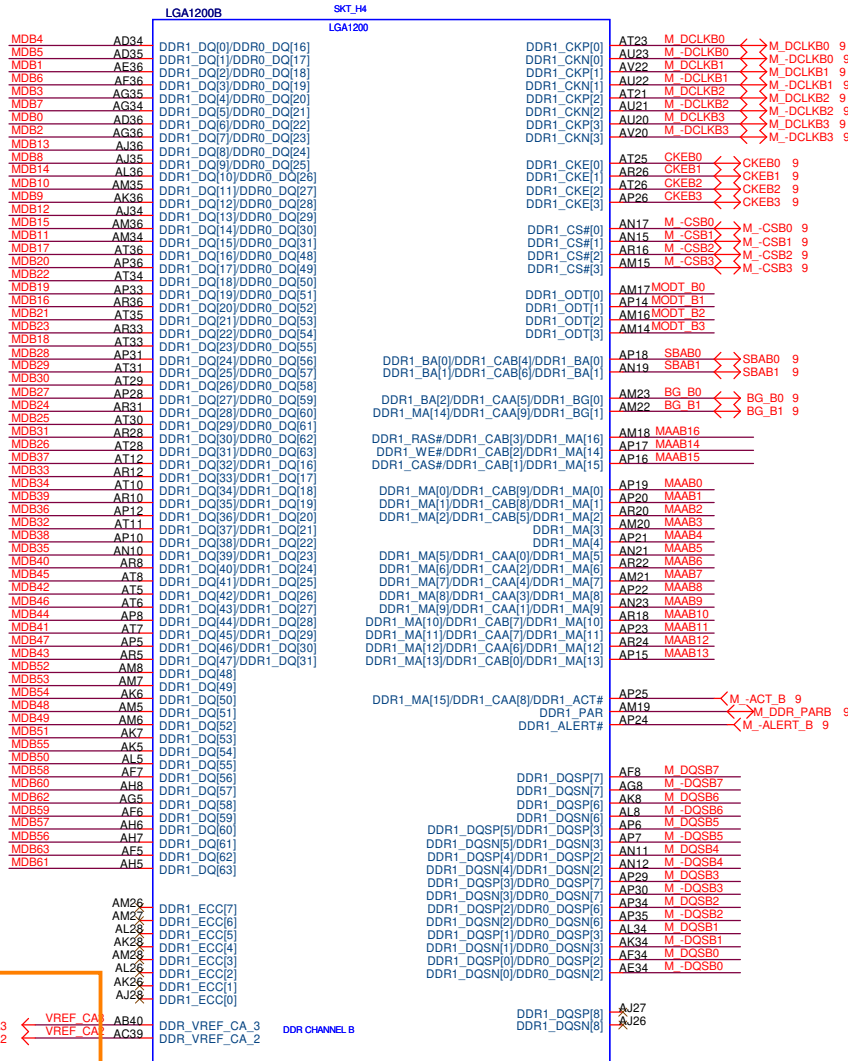
BLOCK DIAGRAM



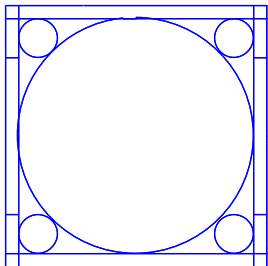




CPU-SK/1200/S/15[10SC1-F01200-11R_10SC1-F01200-12R]

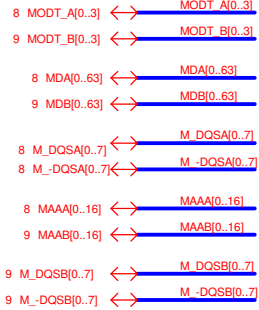
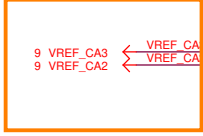


GPU-SK/1200/S/15[10SC1-F01200-11R_10SC1-F01200-12R]



黑色cover

LGA1200
ILM_BP_CR/1200/BKN[12KRC-SF0001-C1R_12KRC-SF0001-C2R]



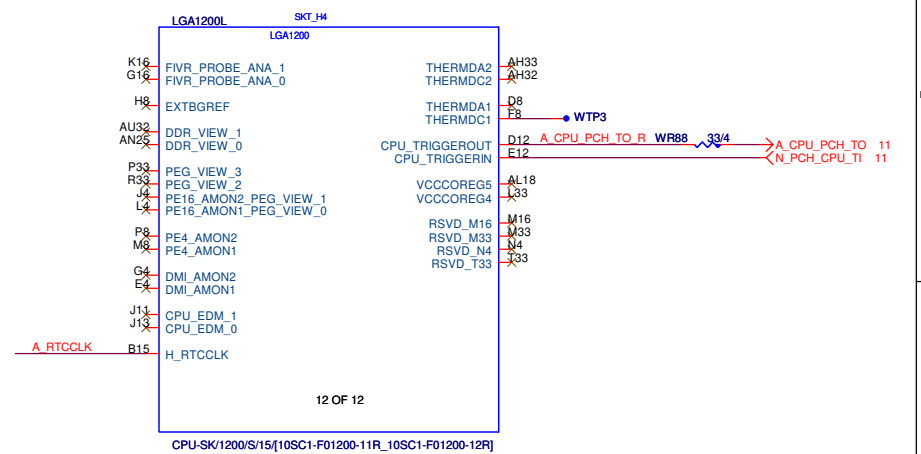
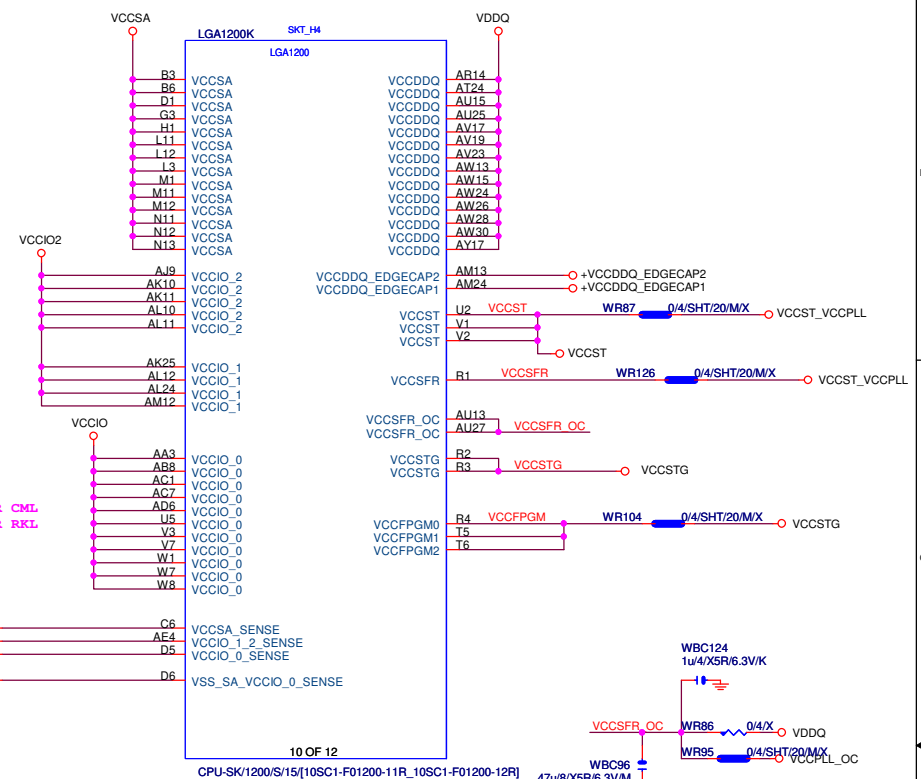
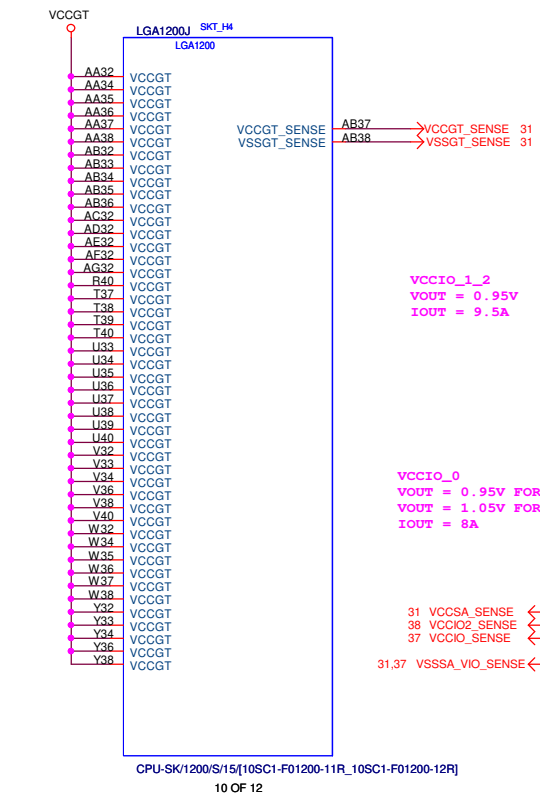
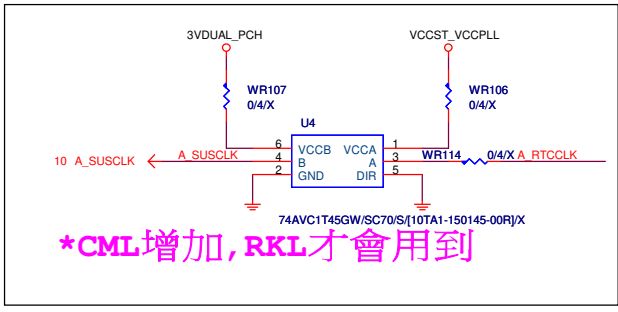
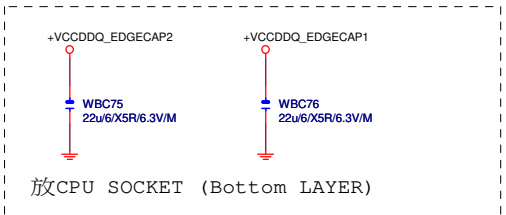
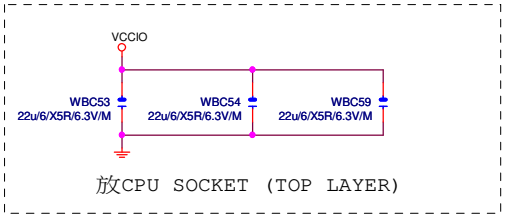
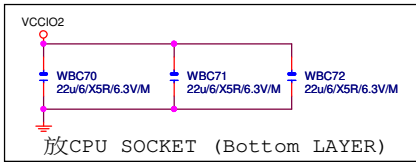
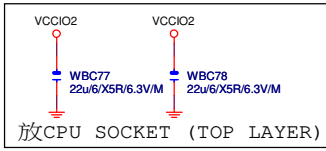
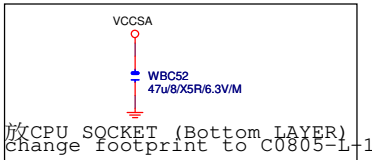
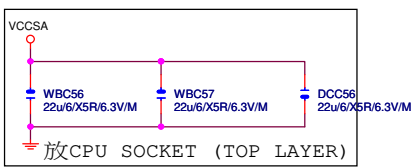
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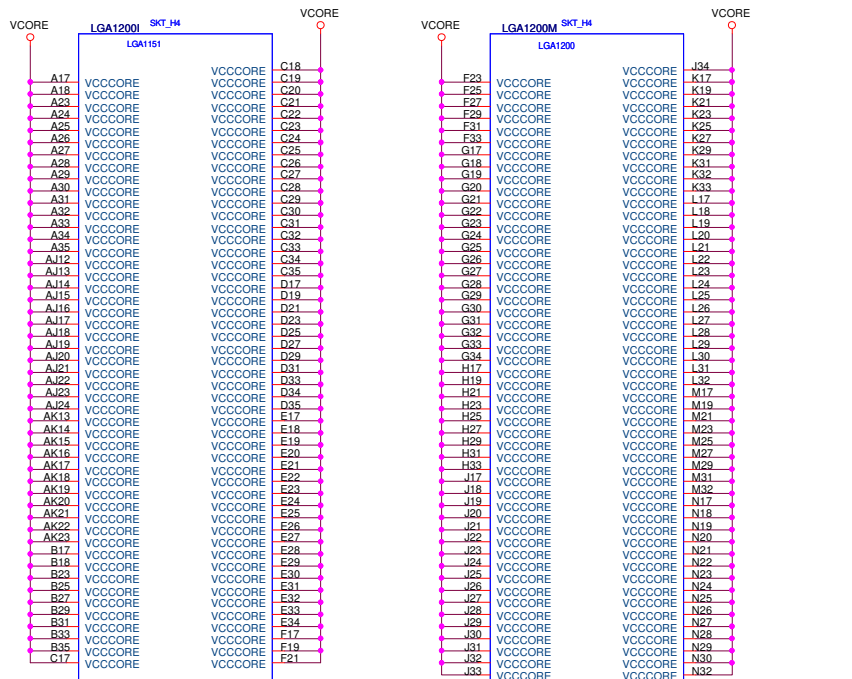
CPU LGA1200-B

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Rev 1.0

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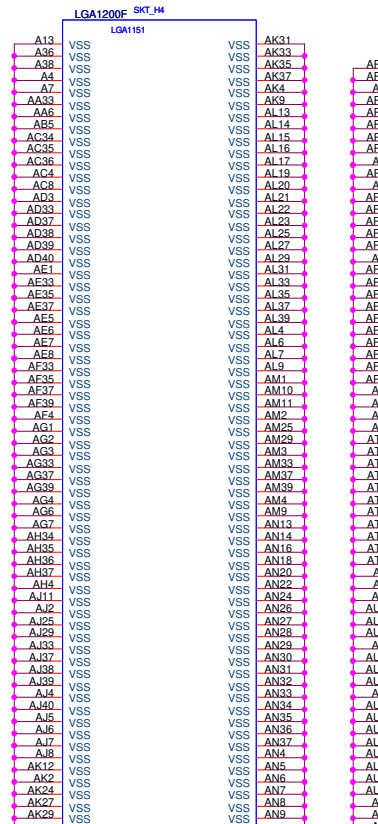


CPU-SK/1200/S/15/[10SC1-F01200-11R_10SC1-F01200-12R]

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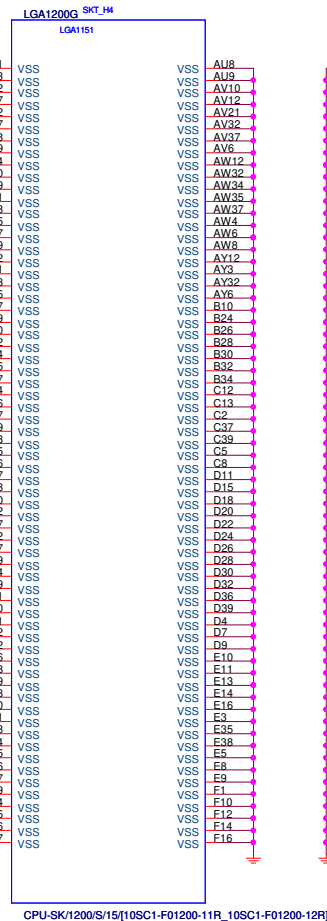
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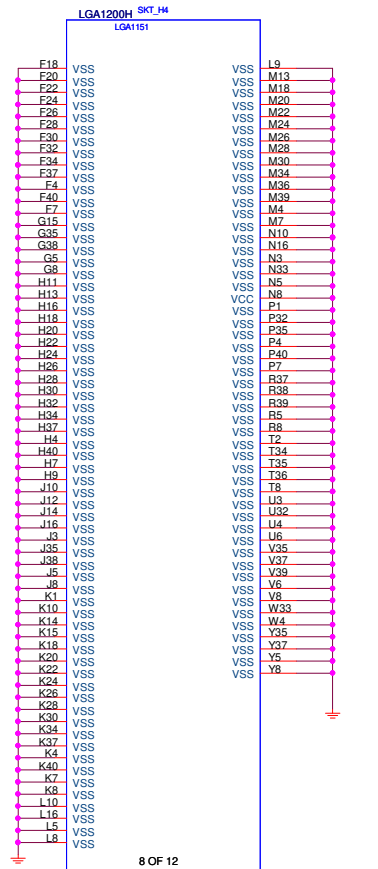
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CPU-SK/1200/S/15/[10SC1-F01200-11R_10SC1-F01200-12R]

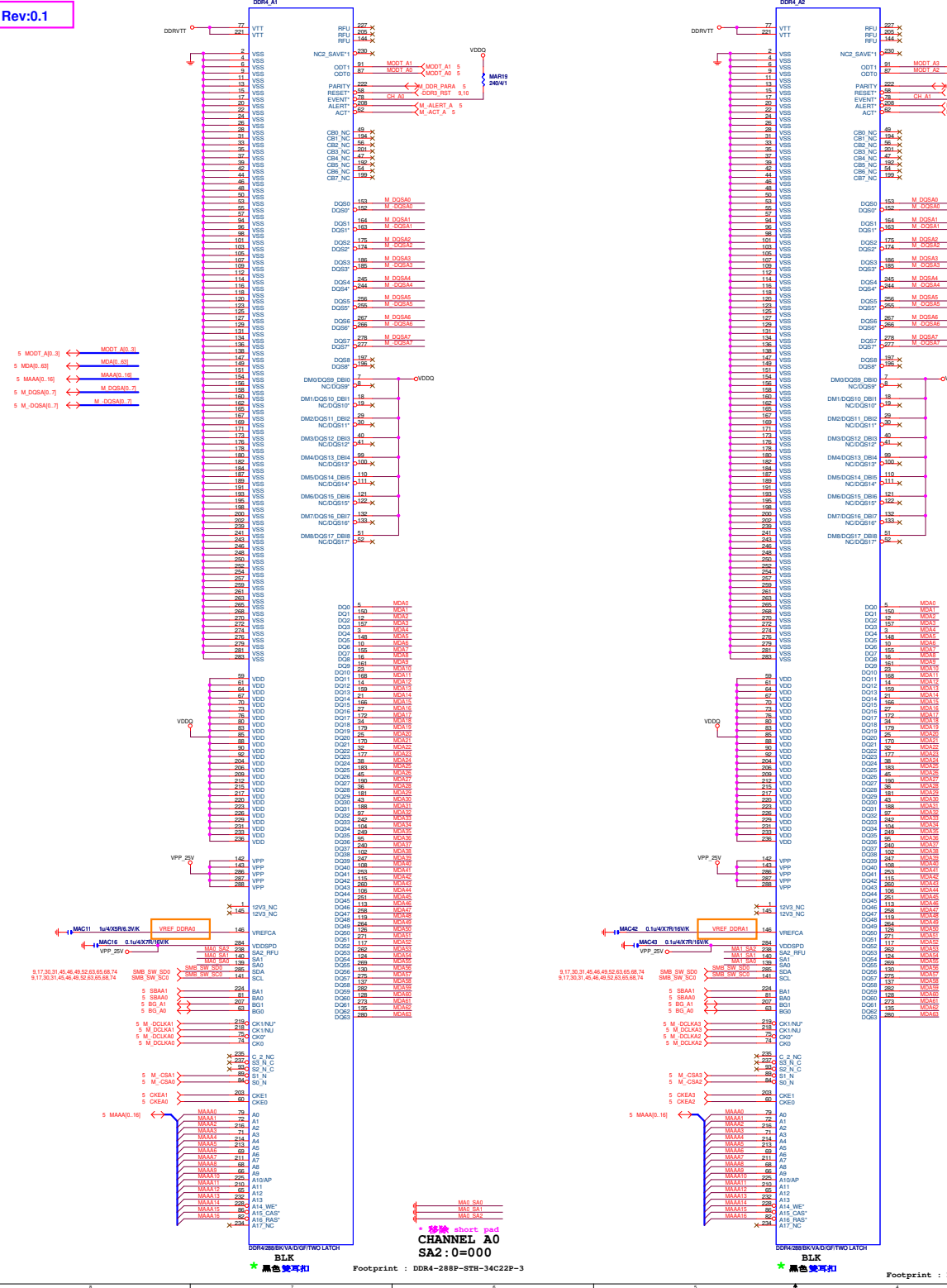
7 OF 12



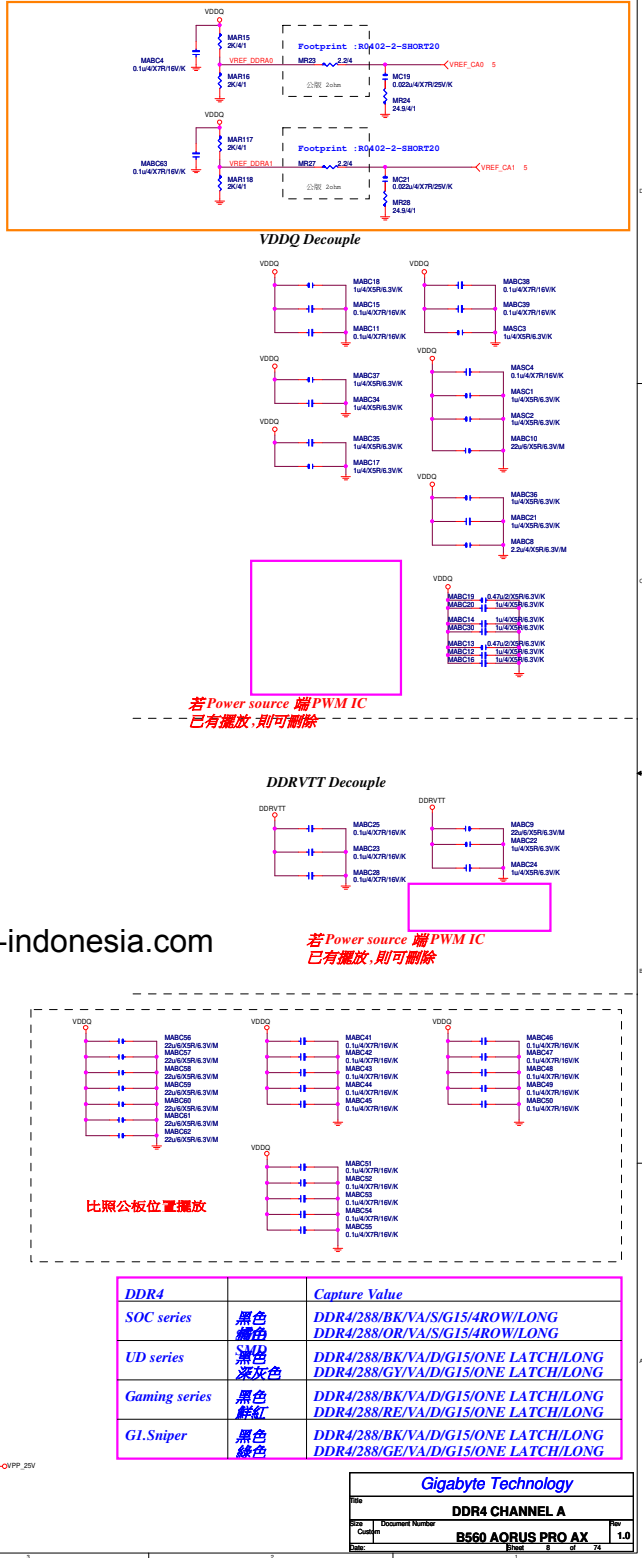
CPU-SK/1200/S/15/[10SC1-F01200-11R_10SC1-F01200-12R]

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* 刪 Vcore 電容



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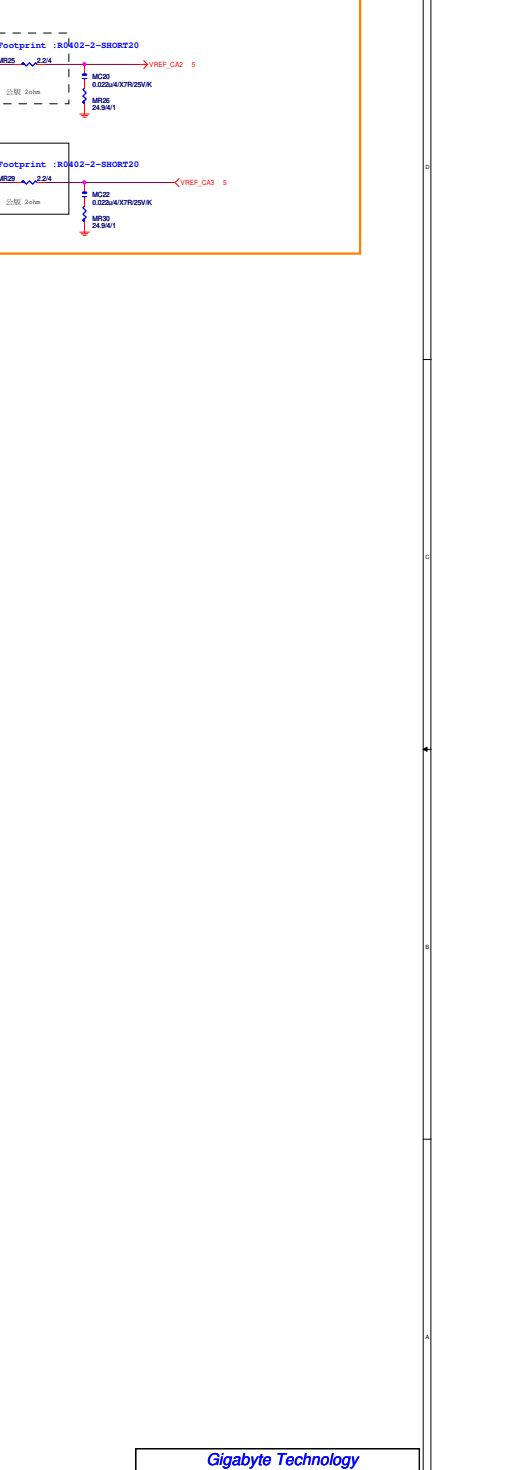
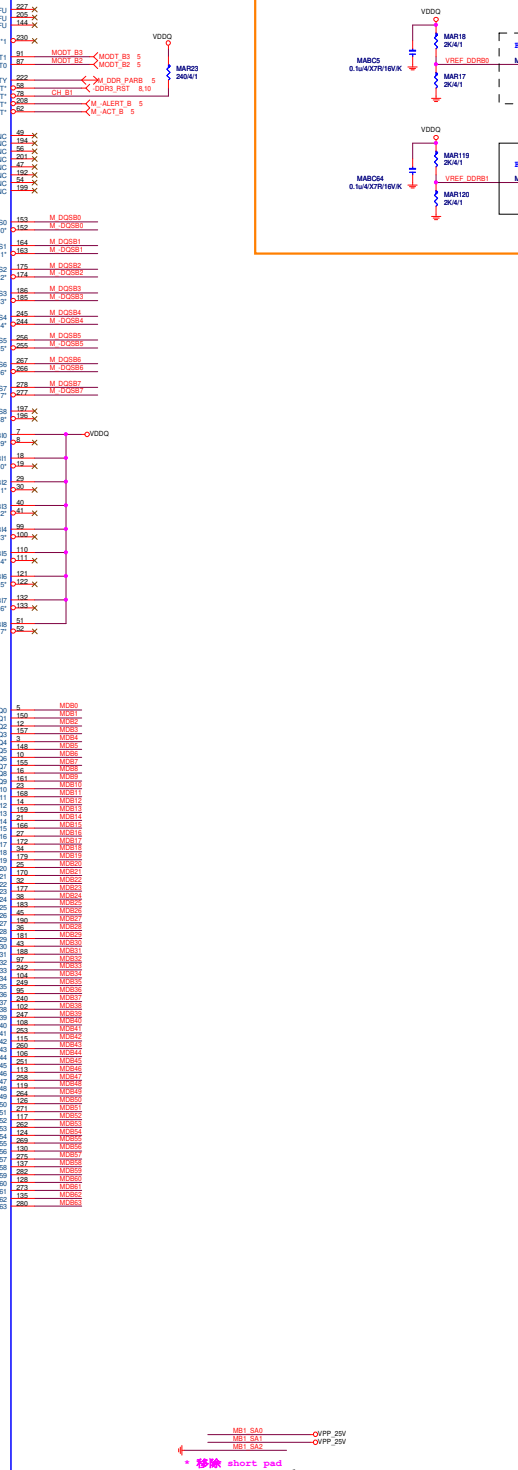
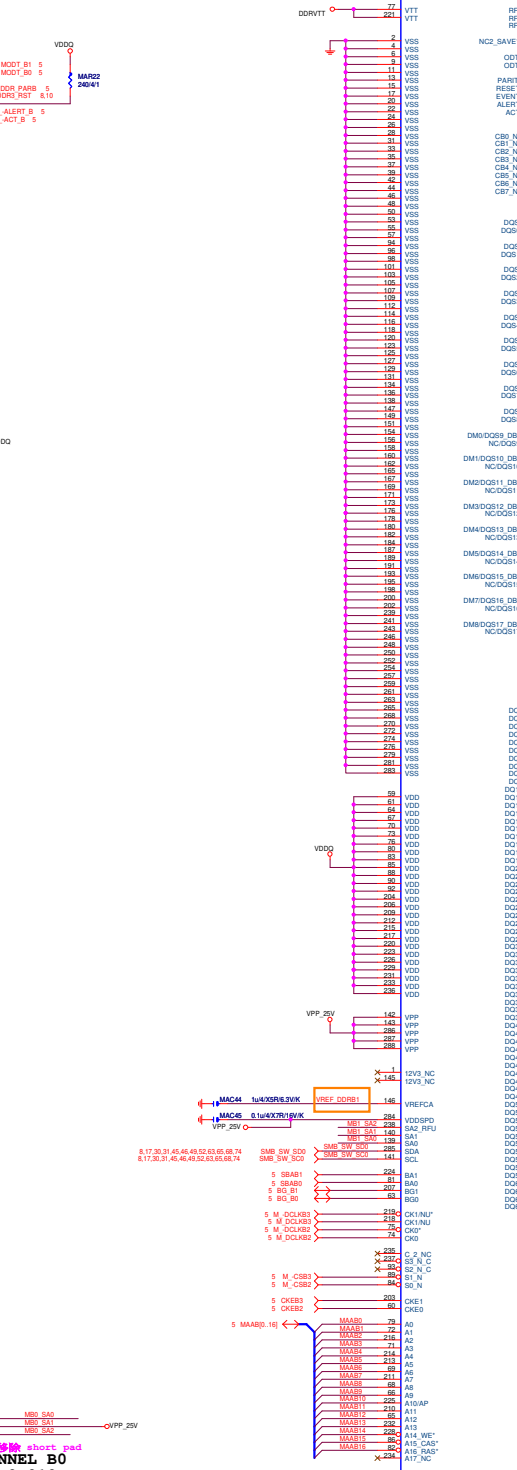
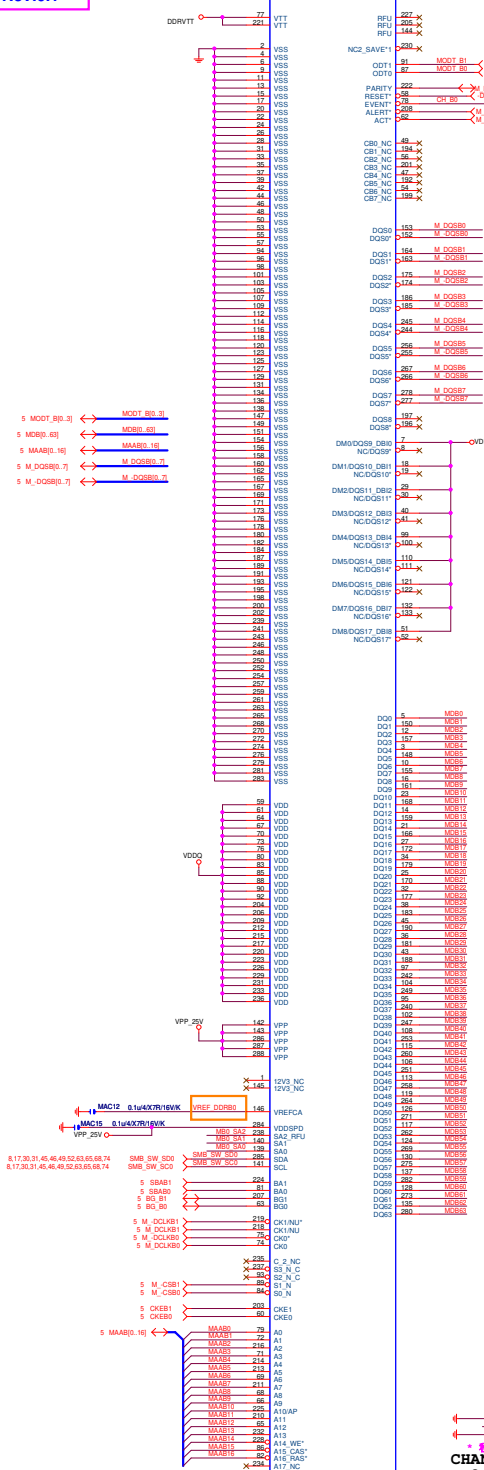
DDR4	Capture Value
SOC series	DDR4/288/BK/VA/S/G15/4ROW/LONG
UD series	DDR4/288/BK/VA/D/G15/ONE LATCH/LONG
Gaming series	DDR4/288/BK/VA/D/G15/ONE LATCH/LONG
Gl.Sniper	DDR4/288/BK/VA/D/G15/ONE LATCH/LONG

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DDR4 CHANNEL A1

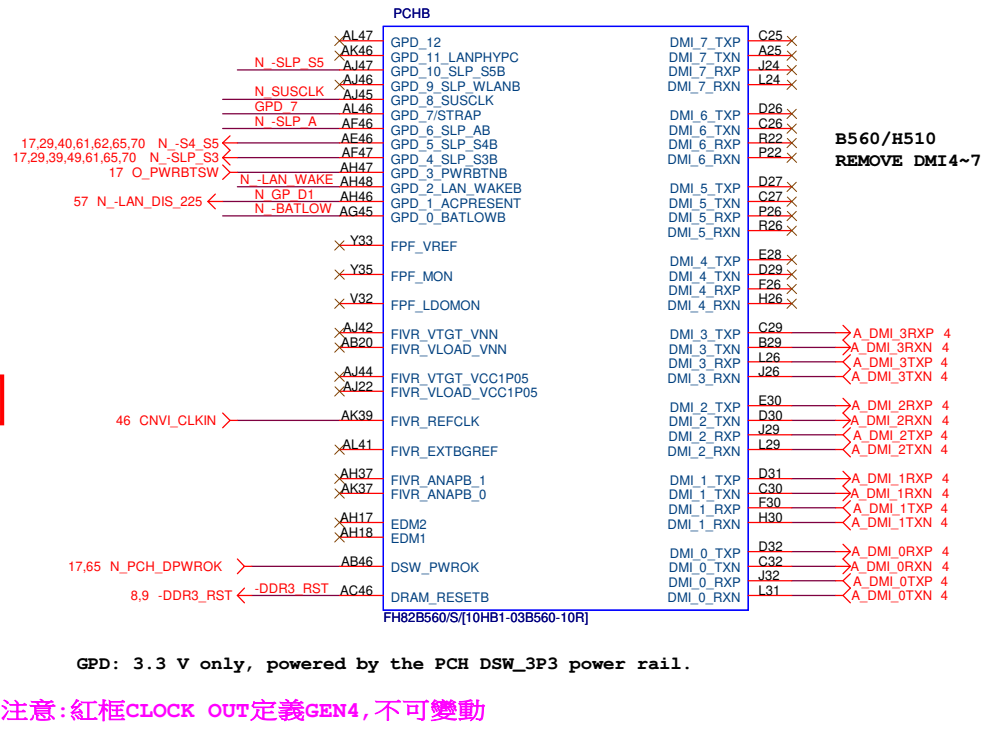
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RKL_TGP_PCH-H R0.1

C10_WAKE RESERVED/BIOS NEED TO PROGRAM
INTERNAL PD ON THIS PIN.



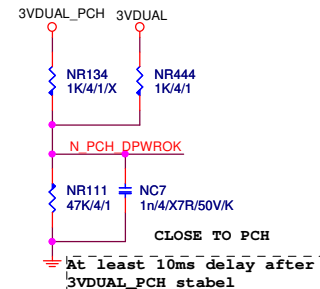
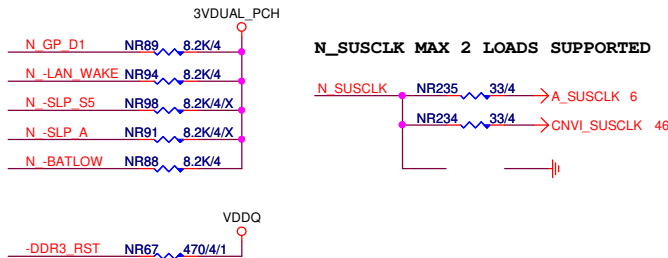
GPD: 3.3 V only, powered by the PCH DSW_3P3 power rail.

**注意:紅框CLOCK OUT定義GEN4,不可變動

CLKOUT_PCIE_P/N [9, 7, 4, 3, 0] = Must be used for PCIe* Gen4 support

STRAP

3VDUAL_PCH
GPD 7 NR237 100K/4X
Reserved. This strap should sample LOW INTERNAL PD.

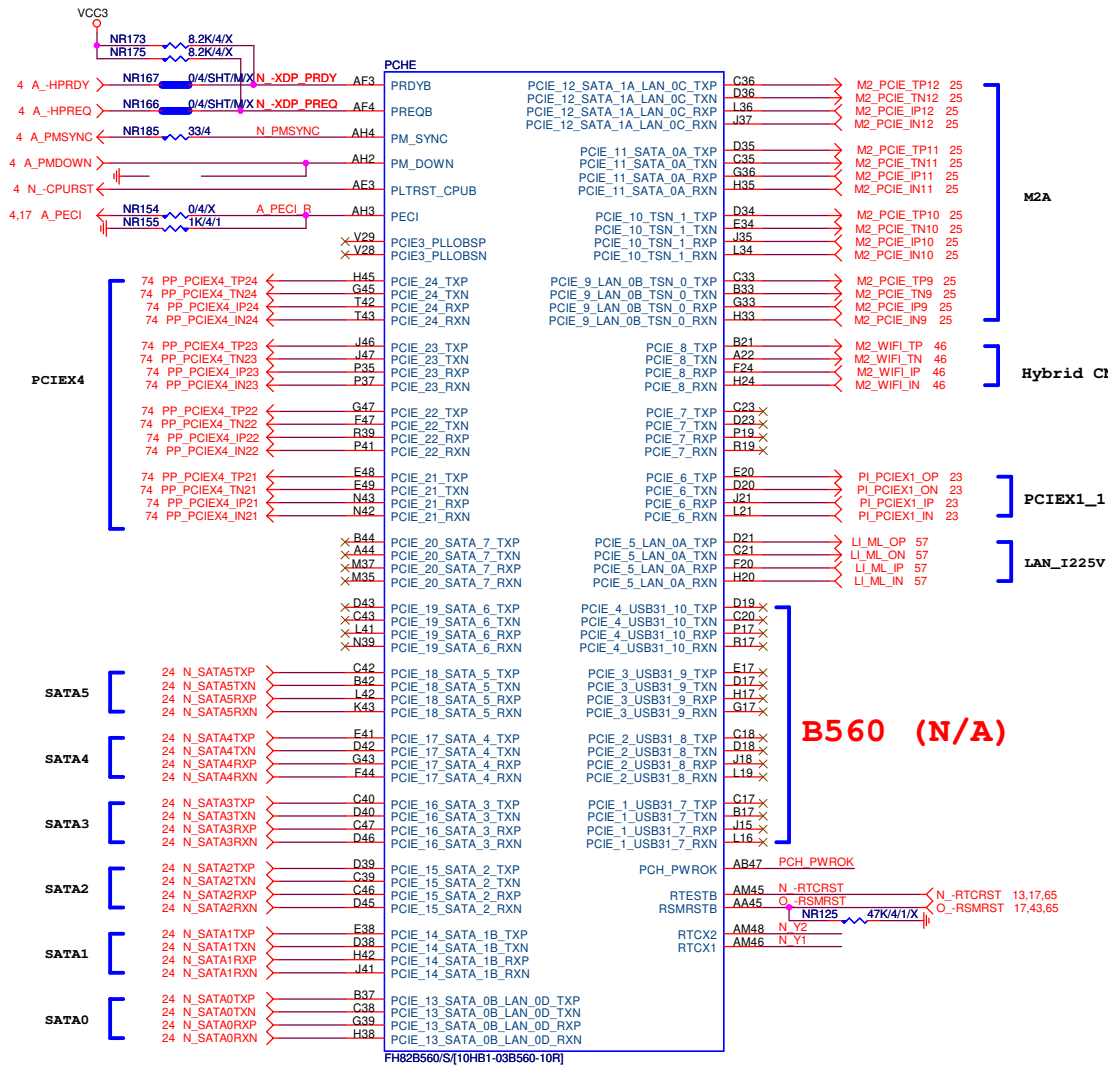


ANS 8680672

Gigabyte Technology

Title		
PCH CLK,DMI,CNVI		
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RKL_TGP_PCH-H R0.1



Intel 500 series PCH PCIE P5-P12							
ITEM	PCIE P5	PCIE P6	PCIE P7	PCIE P8	PCIE P9	PCIE P10	PCIE P11
H510	PCIE /Gbe	PCIE	PCIE	PCIE	Gbe ONLY	N/A	PCIE /Gbe
B560	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE SATA_0'	PCIE SATA_1' Gbe
H570	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE SATA_0'	PCIE SATA_1' Gbe
Z590	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE SATA_0'	PCIE SATA_1' Gbe
Q570	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE SATA_0'	PCIE SATA_1' Gbe
W580	PCIE /Gbe	PCIE	PCIE	PCIE	PCIE /Gbe	PCIE SATA_0'	PCIE SATA_1' Gbe
Intel® RST for x2/x4 M.2							

Intel 500 series PCH PCIE P13-P24											
ITEM	PCIE P13	PCIE P14	PCIE P15	PCIE P16	PCIE P17	PCIE P18	PCIE P19	PCIE P20	PCIE P21	PCIE P22	PCIE P23
H510	SATA_0 /Gbe	SATA_1	SATA_2	SATA_3	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B560	SATA_0 /Gbe	SATA_1	SATA_2	SATA_3	SATA_4	SATA_5	N/A	N/A	PCIE	PCIE	PCIE
H570	PCIE SATA_0 Gbe	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE
Z590	PCIE SATA_0 Gbe	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE
Q570	PCIE SATA_0 Gbe	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE	PCIE	PCIE	PCIE	PCIE
W580	PCIE SATA_0 Gbe	PCIE SATA_1	PCIE SATA_2	PCIE SATA_3	PCIE SATA_4	PCIE SATA_5	PCIE SATA_6	PCIE SATA_7	PCIE	PCIE	PCIE
Intel® RST for x2/x4 M.2						Intel® RST for x2/x4 M.2					

B560 (N/A)

RTC 32.768KHZ

DIP X'TAL

Del DIP NX1

OPTION

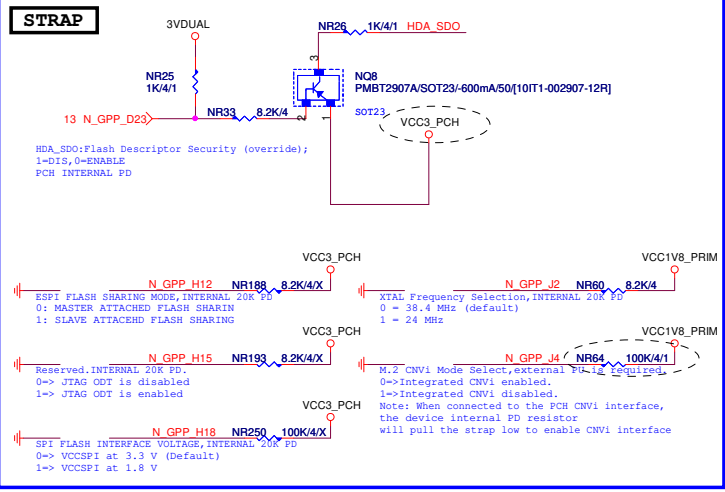
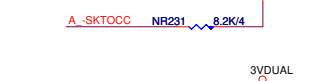
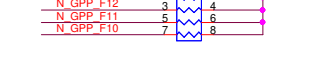
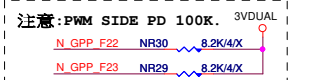
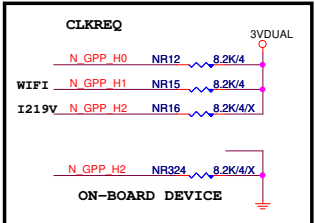
SMD X'TAL

(09/21)intel 500 note item 6

Intel 500 series PCH USB P7-P10				
ITEM	USB P7	USB P8	USB P9	USB P10
H510	NA	NA	NA	NA
B560	NA	NA	NA	NA
H570	U3.2 Gen1x1	U3.2 Gen1x1	PCIE	PCIE
Z590	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1
Q570	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen1x1	U3.2 Gen1x1
W580	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1	U3.2 Gen2x1

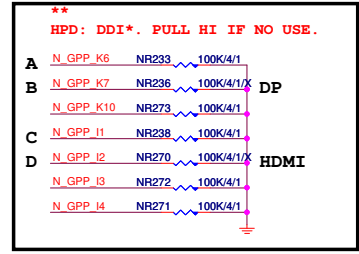
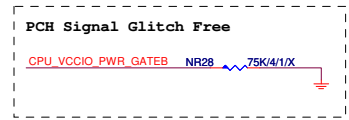
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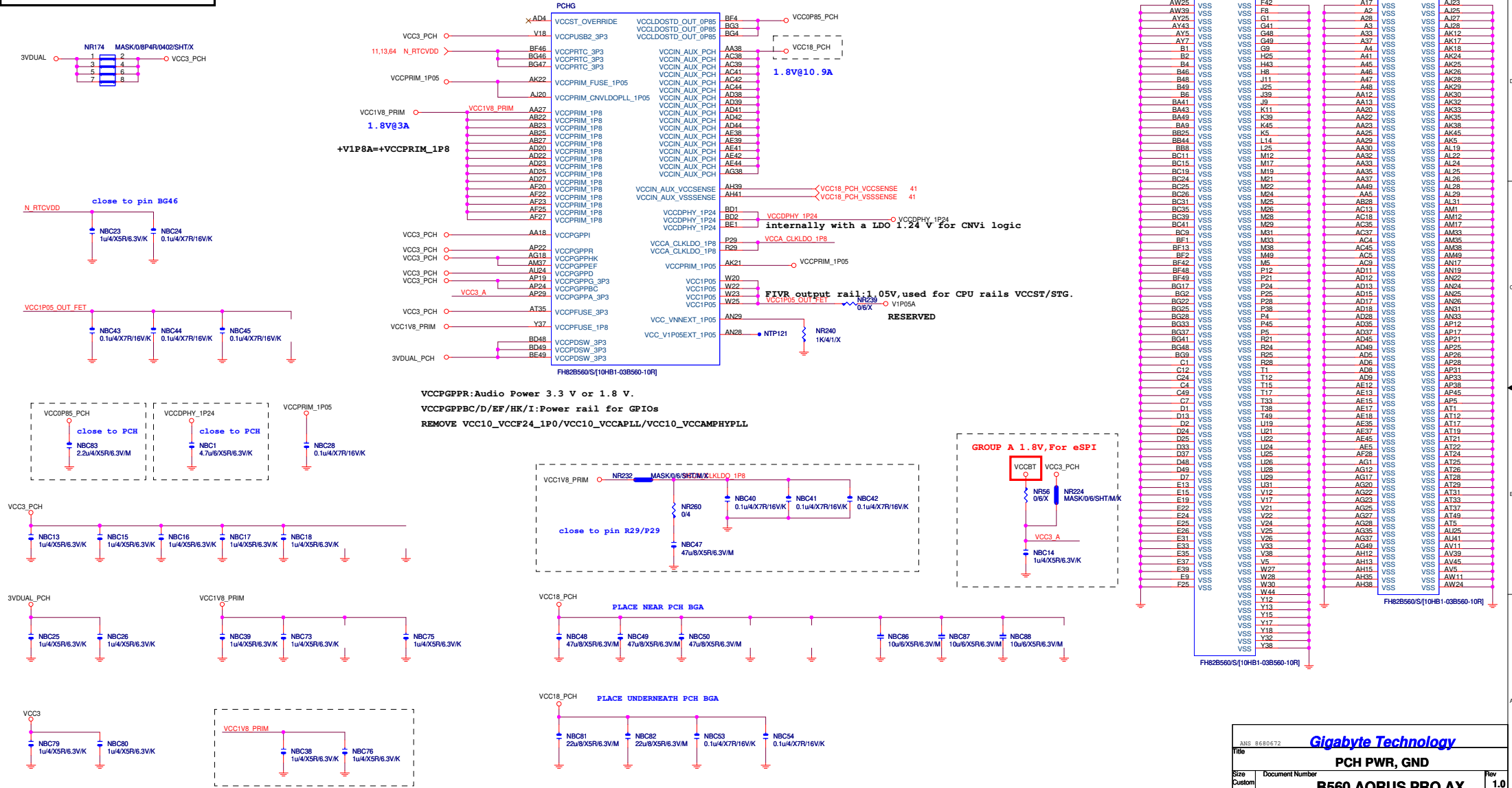
RKL_TGP_PCH-H R0.1



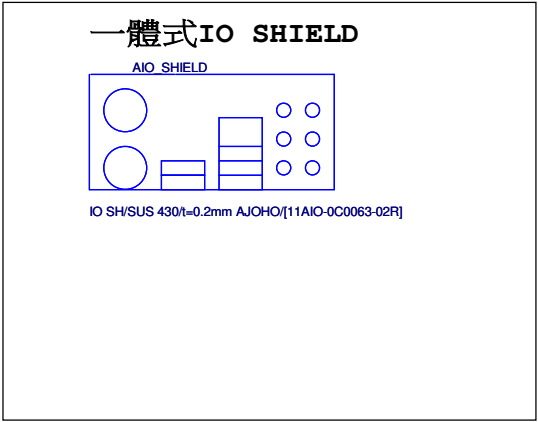
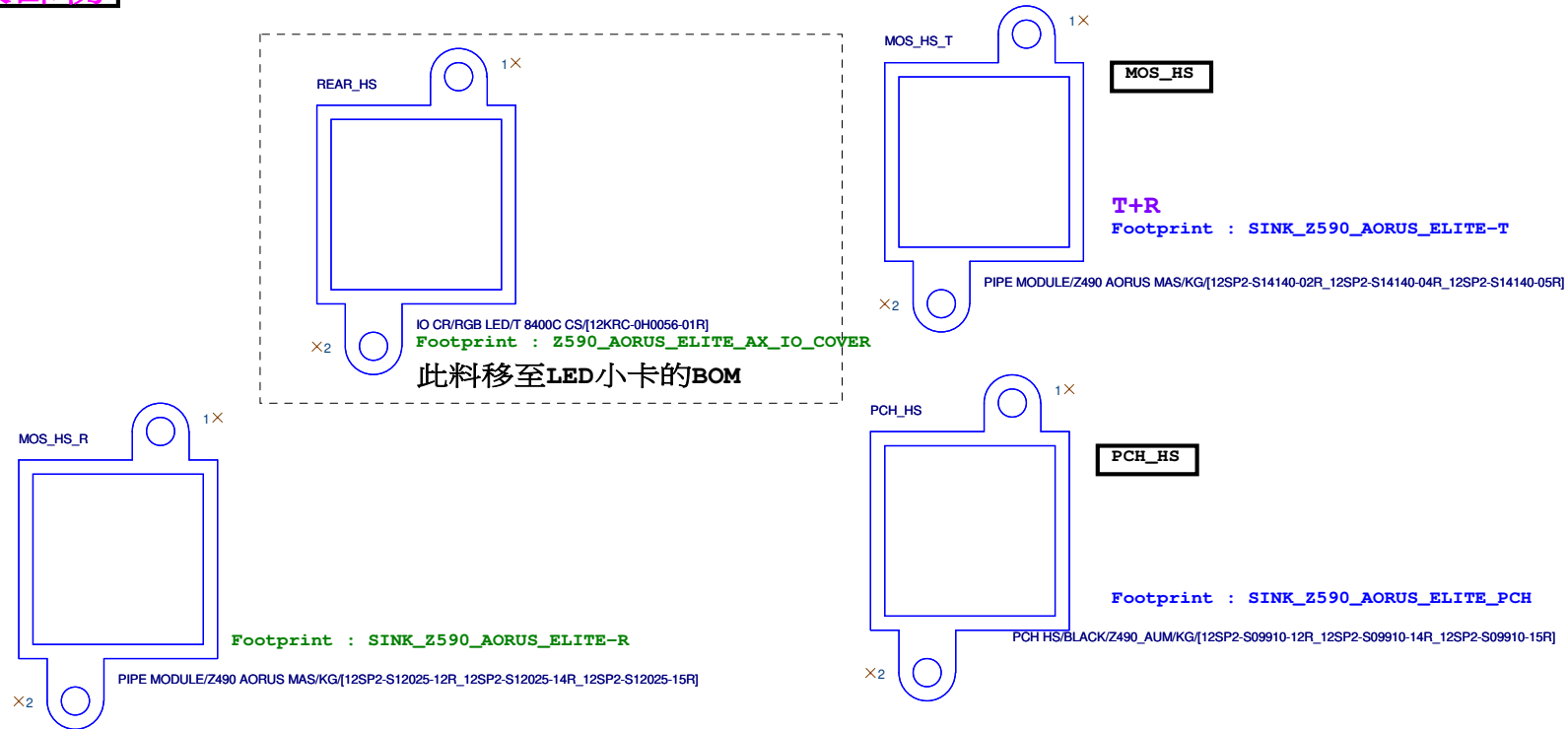
Fixed voltage on certain GPIO groups: GPD (3.3 V), GPP_J and GPP_S (1.8 V/VCCPRIM_1P8)

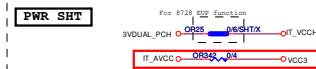
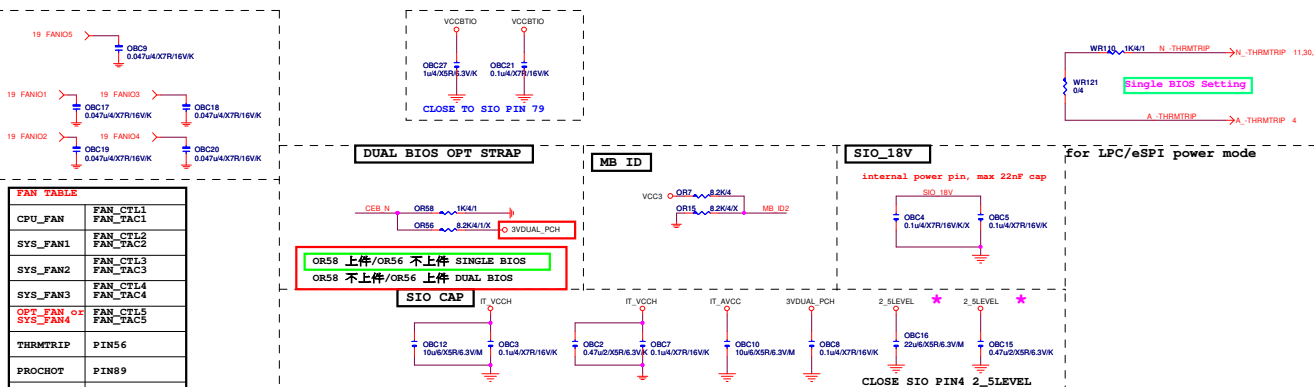
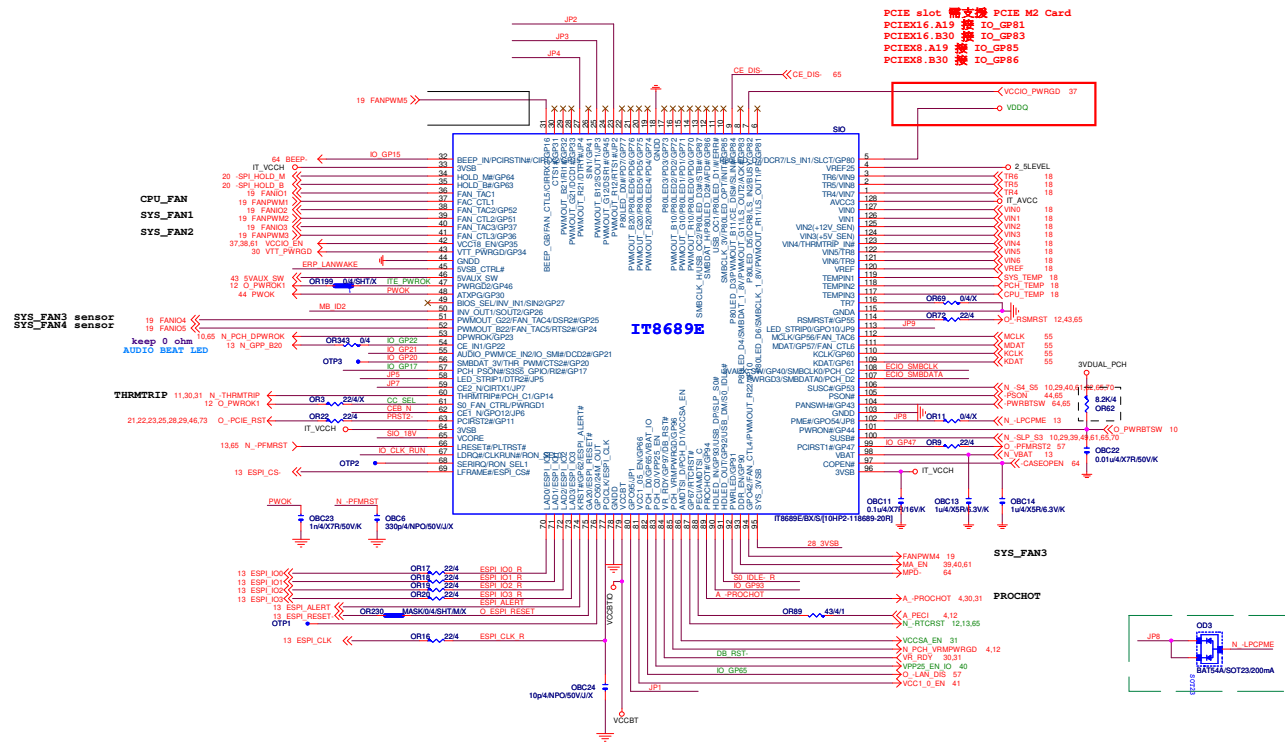
Display Port DDC/HOT PLUG SIGNAL		
CPU PORT	PCH DDC	PCH HPD
DDI_A/EDP	GPP_G0/G1	GPP_K6
DDI_1/B	GPP_I5/I6	GPP_K7
DDI_2/C	GPP_G12/G13	GPP_I1
DDI_3/D	GPP_G14/G15	GPP_I2



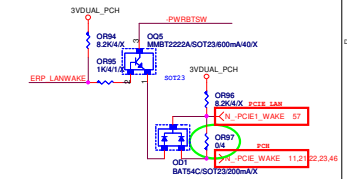


裝甲HEATSINK 分成四大部份



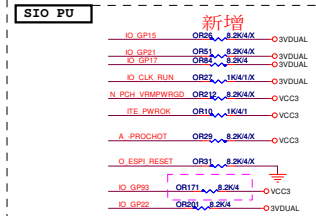


請依開案規格，選擇Support Exp下 LAN Wake up組態。

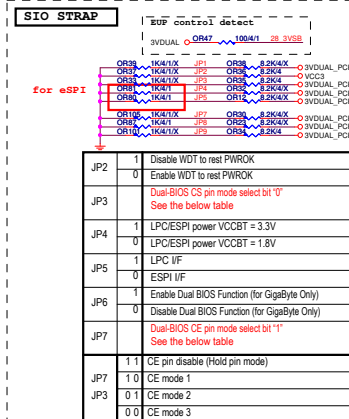


(組態一) PCIE LAN(Single & Dual LAN)

(組態二) INTEL219 LAN(Single LAN)



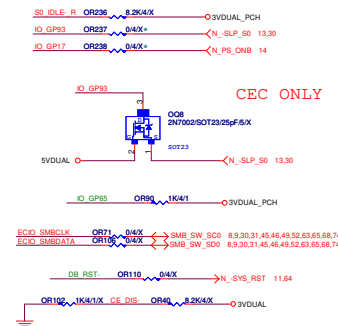
SIO PU



SIO STRAP

for eS

JP2	1	Disable WDt to rest PWROK
	0	Enable WDt to rest PWROK
Dual-BIOS CS pin mode select bit "0" See the below table		
JP4	1	LPC/ESPI power VCCB2 = 3.3V
	0	LPC/ESPI power VCCB2 = 1.8V
JP5	1	LPC IF
	0	ESPI IF
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
Dual-BIOS CE pin mode select bit "1" See the below table		
JP7	1 1	CE pin disable (Hold pin mode)
	1 0	CE mode 1
JP3	0 1	CE mode 2
	0 0	CE mode 3




ERP WOME on LAN		
Single LAN	Realtek	組態一
	Atheros	
	Intel 219	組態二
Dual LAN 只有一個 LAN 交換器 ERP 下 WOME 可用	Atheros+Atheros	組態一
	Intel 219+Atheros	組態三
	Intel 219+Intel 210	
No Support	Single LAN WOME 只上 OR97。 Dual LAN WOME 只上 OR97、OR99。	

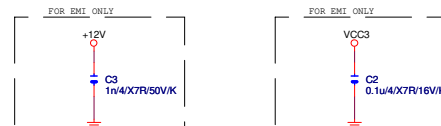
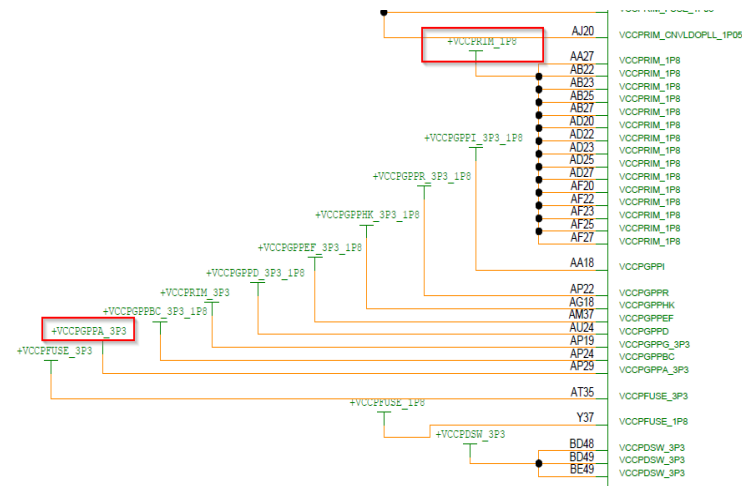
Gigabyte Technology			
Title			
IT8688			
Size	Document Number		Rev
Custom	B560 AORUS PRO AX		1.0
Date:	Wednesday, January 27, 2021		Page 17 of 74

The schematic diagram illustrates the temperature sensor circuit. It features a VREF pin connected to a network of resistors (OR73, R674, R675) and capacitors (OC7, OC6, OC16). The circuit also shows connections for SYS_TEMP, CPU_TEMP, and PCH_TEMP pins, with labels for 'Close S10' and 'Close P1' indicating specific connection points or components.

[illegible][illegible]

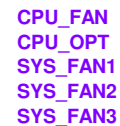


Pin	Mode	Configuration
JP4 HI	ESPI MODE	VCCBT 3.3V
JP5 HI	ESPI MODE	LPC I/F
JP4 LO	ESPI MODE	VCCBT 1.8V
JP5 LO	ESPI MODE	ESPI I/F



Gigabyte Technology

Title				HWM,KB/MS, FAN CTRL			
Size	Document Number						Rev
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[illegible]

CPU_OPT

17 FANPWM5

13 N_GPP_B17

VCC3

FGR1 1K4/1

FGR2

100K/4/1

FGC1 0.1u4/X7R/16V/K

FGC3 10u8/X5R/16V/K

+12V

FANPWM5

FAN7DCIN

FAN7_MODE

FGDU1

NCT3947S/SOP8-EP

VIN

PWMOUT

VOUT

CFAN7_PWMOUT

CFAN7_VOUT

PWMIN

DCIN

NC

NC

MODE

PGND

FGC2 10u8/X5R/16V/K

CFAN7_VOUT

COPT_3

CFAN7_PWMOUT

CPU_OPT FAN1*4/BK/A3/PA66

+12V

FGR3 3.3K/4/1

FGR4 15K/4/1

FANIOS

FGR5 6.2K/4/1

17

**MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.**

SYSTEM FAN2

VCC3

FBR1 1K/4/1

17 FANPWM3

FBR2

100K/4/1

0.1u/4X7R/16V/K

FBC1

0.045H/10M/X

13 N_GPP_B15

MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.

+12V

FBC3

10u/8X5R/16V/K

FBDU1

5 VIN

2 PWMOUT

4 FAN2_VOUT

1 FANPWM3

PWMIN

8 FAN2DCIN

DCIN

6 FAN2_MODE

MODE

PGND

9

NCT3947S/SOP8-EP

+12V

FBR3 3.3K/4/1

SFAN2_3

FAN2_VOUT

FAN2_PWMOUT

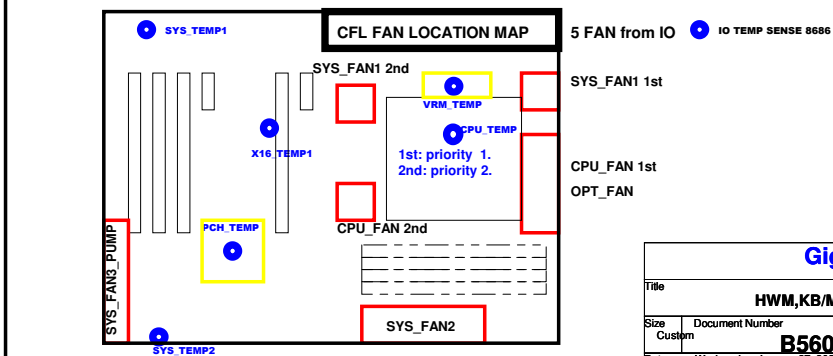
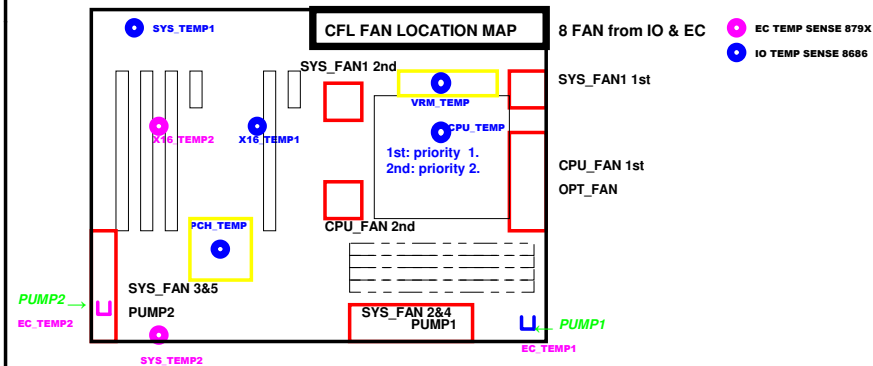
FBR4 15K/4/1

FAN114/BK/A3/PA66

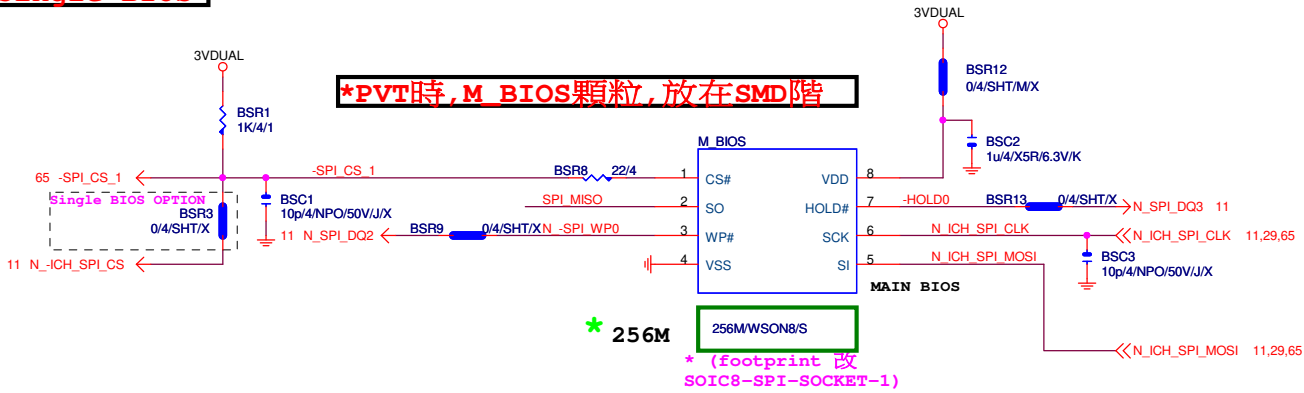
FAN1

FBR5 6.2K/4/1

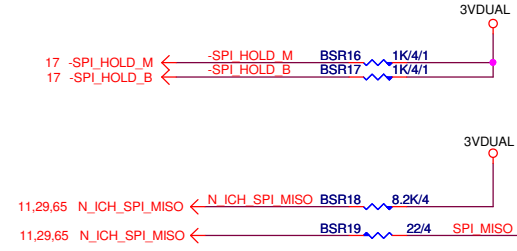
FANIO3 17

[illegible]

DUAL BIOS *Single BIOS

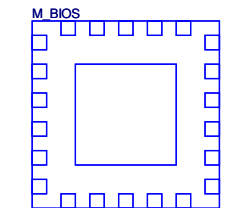


MOSI For DMI RX Termination Voltage



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K



LCP/G-FL/1.27mm/200MIL/WHITE[10SL2-000008-71R]/X

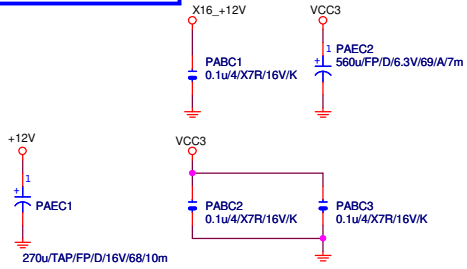
* 試產先上, PVT 移除

Rev 0.3

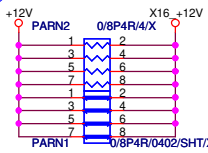
PCIEX16 CAP

PCIEX16 SLOT

PCIESLOT-1645TH



PCIEX16 PROTECT SHT

+12 protect
short-wire test

PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC21	0.22u4/X5R/6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC20	0.22u4/X5R/6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R/6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R/6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R/6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R/6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R/6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R/6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R/6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R/6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R/6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R/6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R/6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R/6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R/6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R/6.3V/K	PA EXP TXN15 C

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b) X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b) X16=32Gb/s=4GB/s

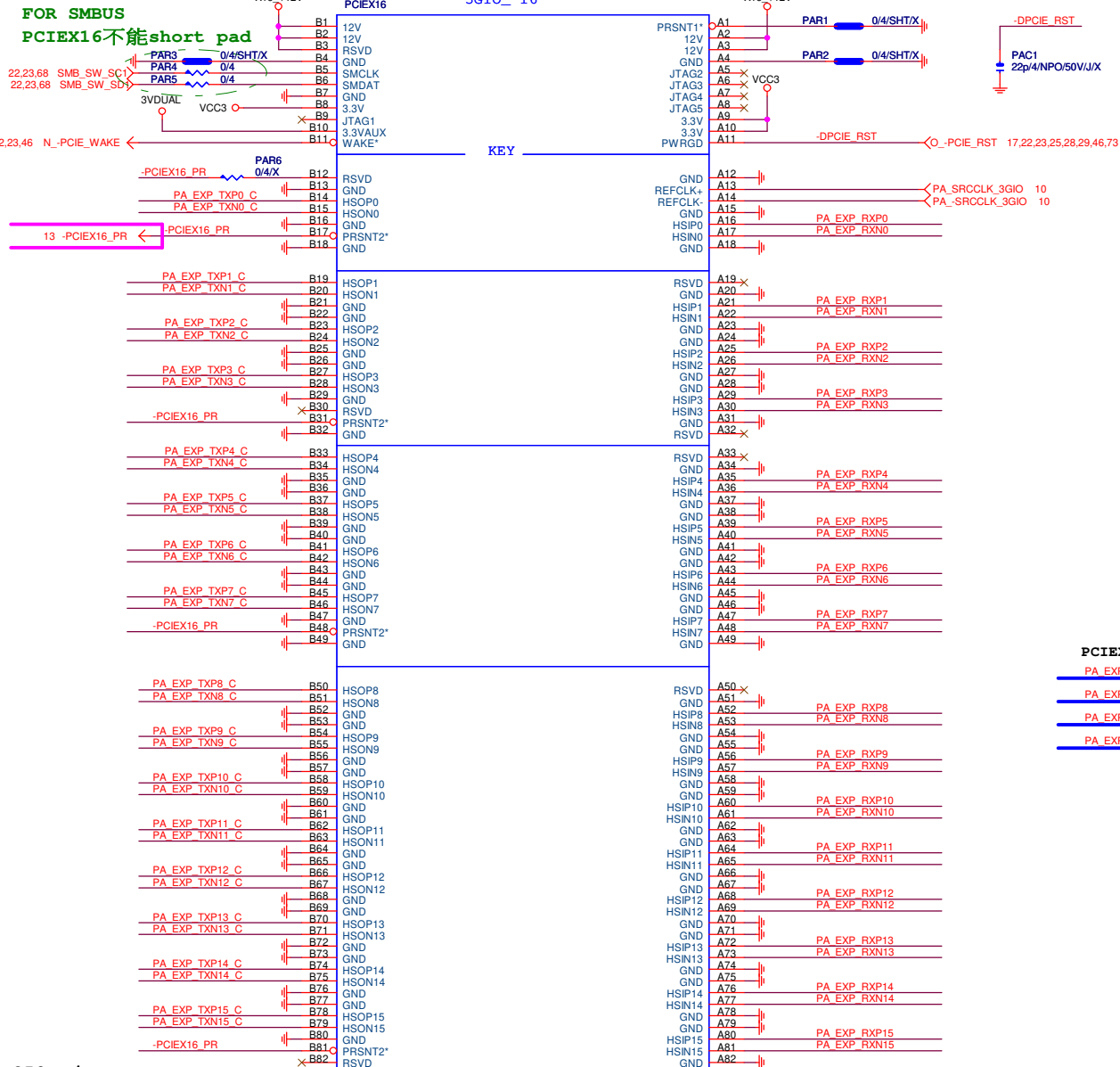
PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b) X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

PCE-E X1(單向) BANDWITH=5GHz*(8b/10b)=4Gb/s=500MB/s

PCI-E REV:3.0--> 8GHZ

PCE-E X1(單向) BANDWITH=8GHz*(128b/130b)=8Gb/s=1GB/s



PCI-E16X-164P/BK/LONG DOUBLE/HK*2/SHELL/GEN4.0[11AC1-023164-V2R]

黑色 金屬加強

PCIEX16:16/5/5/5/16

PA EXP RXP[0..15] >>> PA_EXP_RXP[0..15] 4
PA EXP RXN[0..15] >>> PA_EXP_RXN[0..15] 4
PA EXP TXP[0..15] >>> PA_EXP_TXP[0..15] 4
PA EXP TXN[0..15] >>> PA_EXP_TXN[0..15] 4

Gigabyte Technology

PCI EXPRESS * 16

Title	Document Number	Rev
	B560 AORUS PRO AX	1.0
Size	Custom	
Date:	Wednesday, January 27, 2021	Sheet 21 of 74

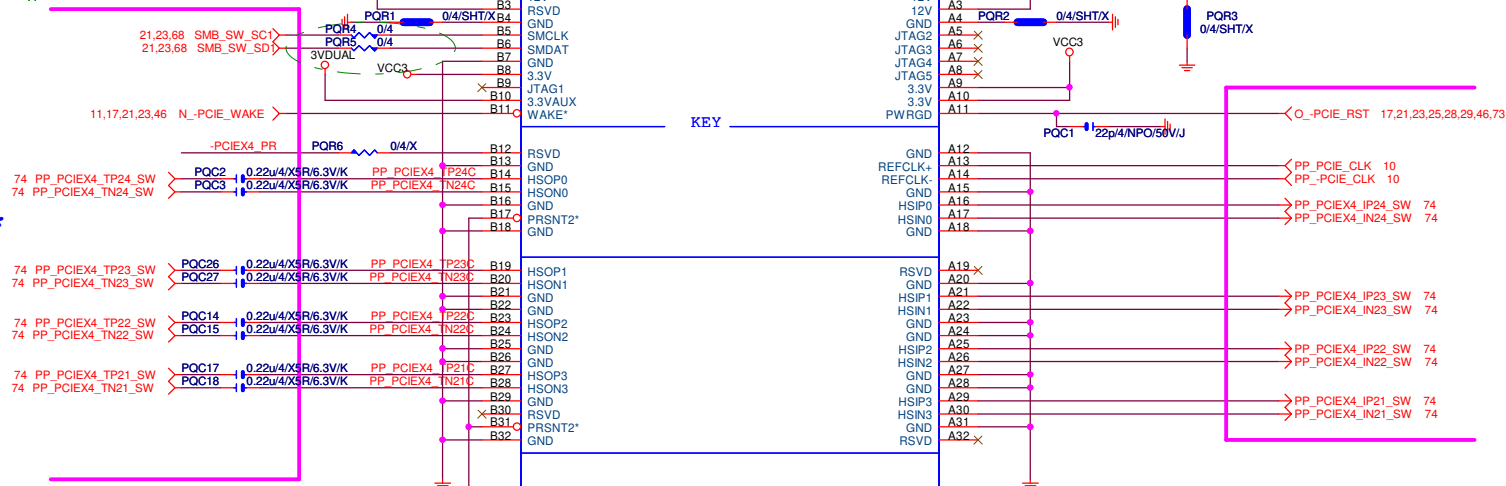
Rev 0.51

PCIE*4

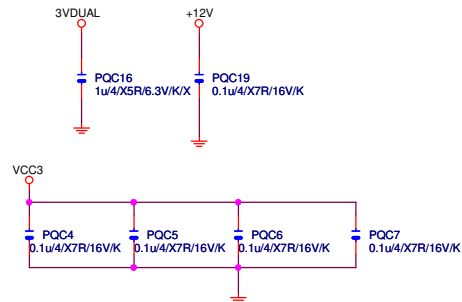
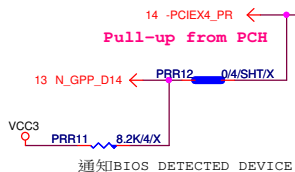
★ Footprint "PCIESLOT-64STH-1"

FOR SMBUS

PCIE4 SM Bus电阻layout 改0 ohm
上件



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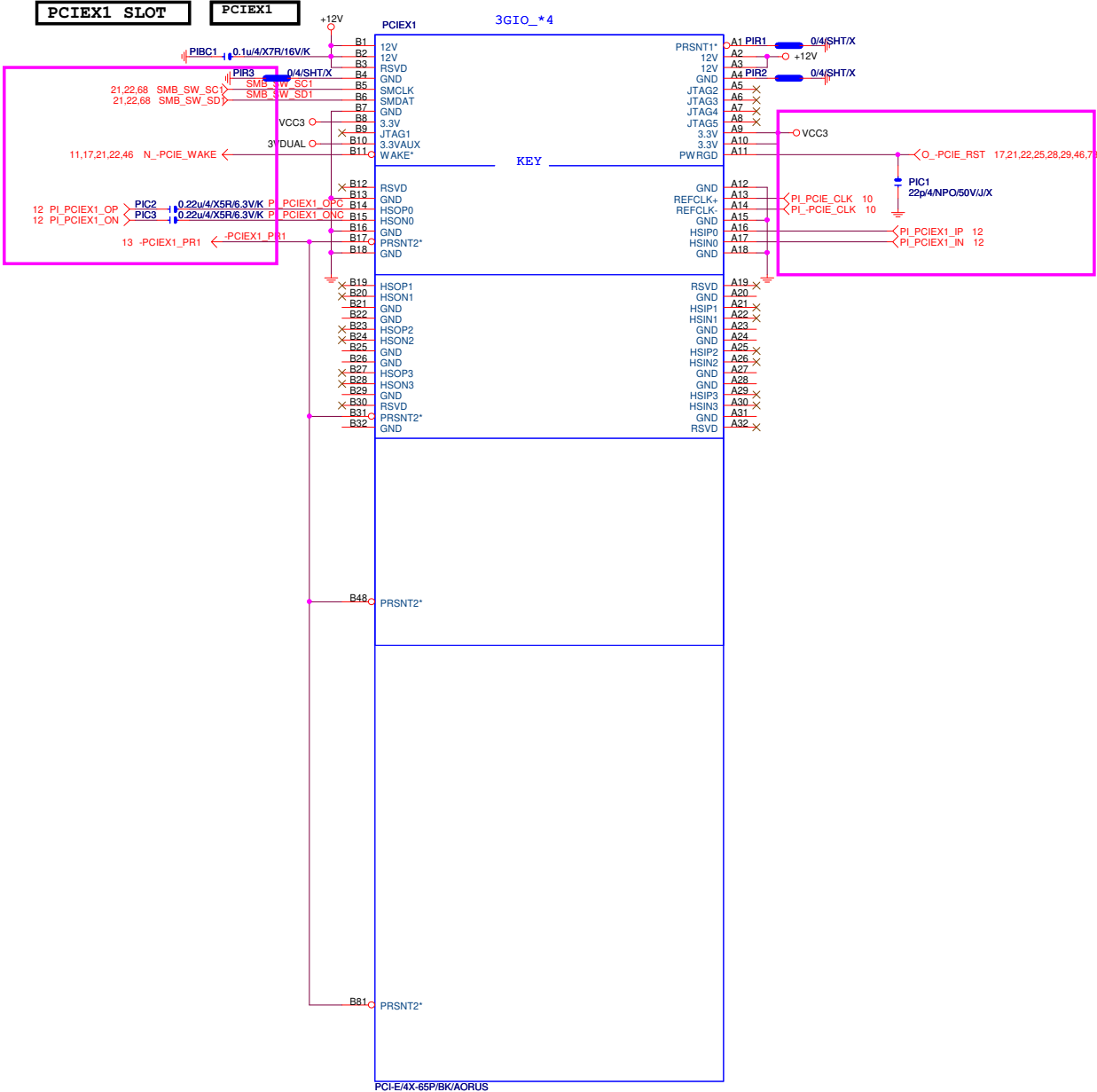


黑色

Gigabyte Technology

Title			
PCIE X4			
Size	Document Number	Rev	
Custom	B560 AORUS PRO AX	1.0	
Date:	Wednesday, January 27, 2021	Sheet	22 of 74

Rev 0.51



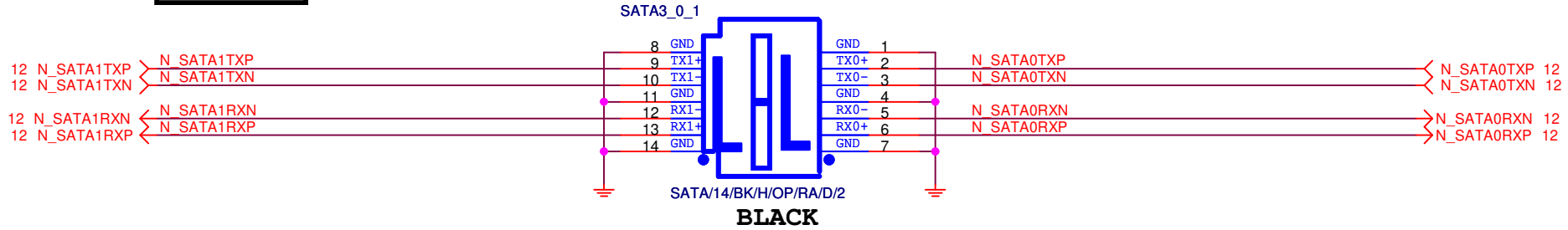
IO18/IO19 To SATA3 port0/1

6 SATA3 from Z490 (90度R-A)

SATA3 0/1

上 Port (8~14)

下 Port (1~7)



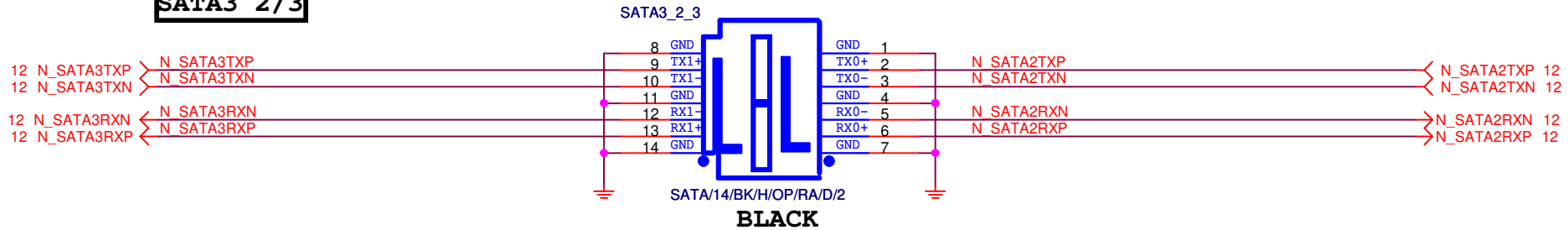
Footprint : H2X7-SATA2-D90

IO20/IO21 To SATA3 port2/3

上 Port (8~14)

下 Port (1~7)

SATA3 2/3



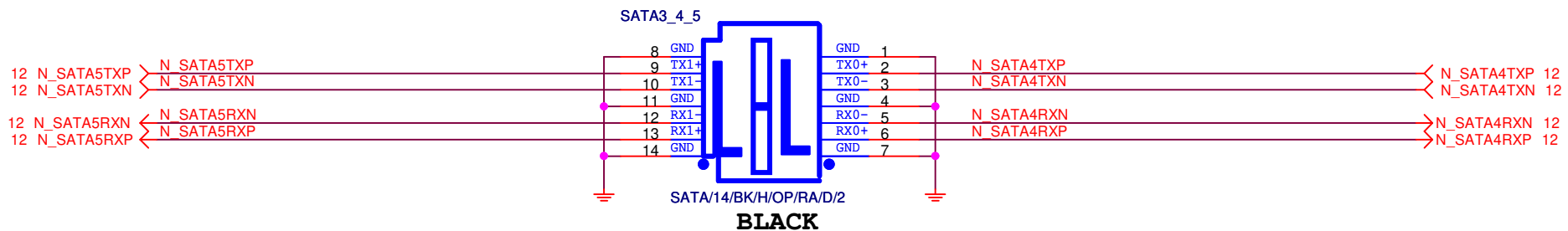
Footprint : H2X7-SATA2-D90

IO22/IO23 To SATA3 port4/5

上 Port (8~14)

下 Port (1~7)

SATA3 4/5



Footprint : H2X7-SATA2-D90

Gigabyte Technology

Title		
SATA		
Size	Document Number	Rev
Custom	B560 AORUS PRO AX	1.0
Date:	Wednesday, January 27, 2021	Sheet 24 of 74

Rev 0.1

M.2 Lane4 from PCH port9

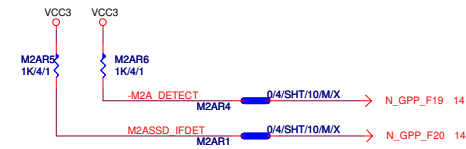
M.2 Lane3 from PCH port10

M.2 Lane2 from PCH port11

M.2 Lane1 from PCH port12

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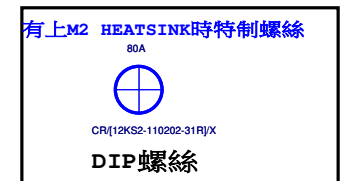
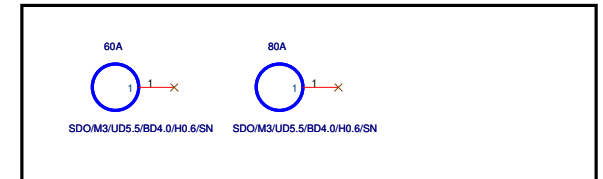
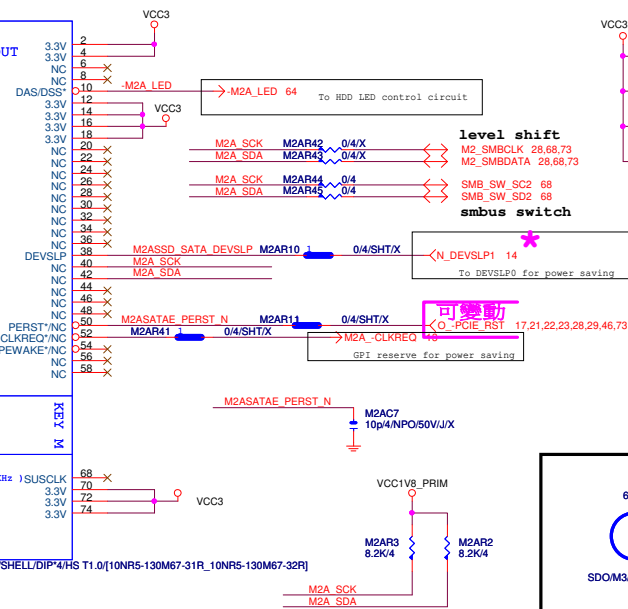
支援SATA and M.2 function



架高

Footprint : M2_110_H2MM8W

Flex IO priority	N_GPP_K1	IO14 PCIe#9	IO15 PCIe#10	IO16 PCIe#11	IO17 PCIe#12
M2A SATA	L	PCIE	PCIE	SATA 0	SATA 1
M2A PCIE (PCIE Reverse)	H	PCIE	PCIE	PCIE	PCIE



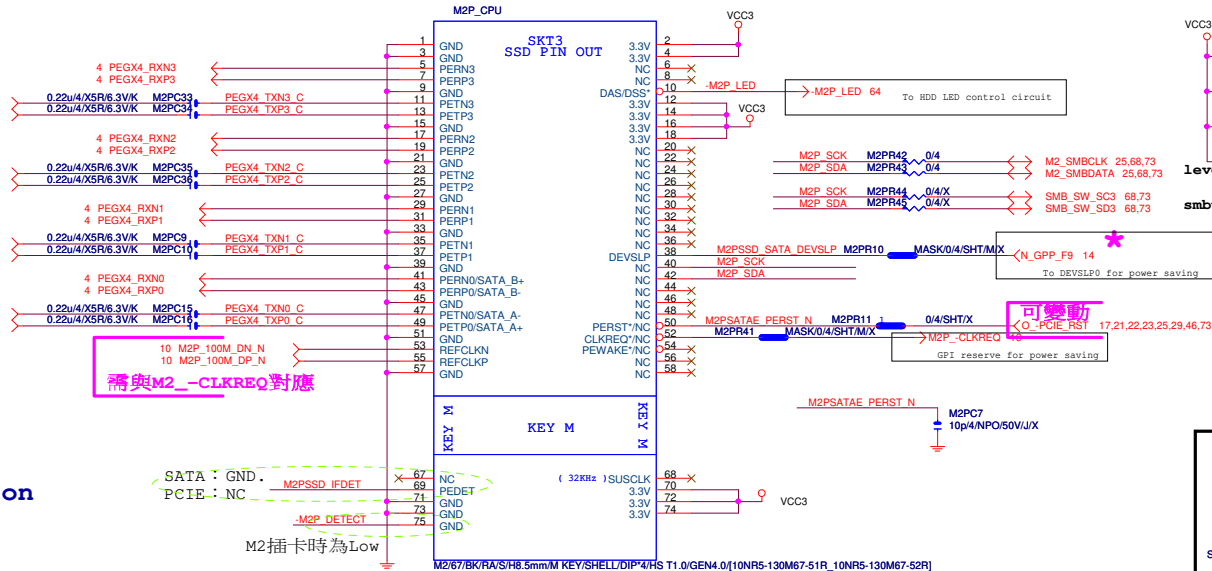
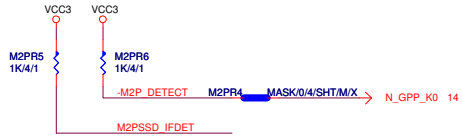
Rev 0.1

M.2 Lane4 from CPU port4

M.2 Lane3 from CPU port3

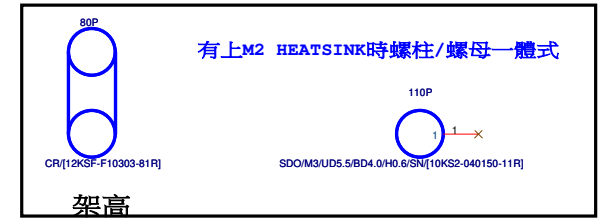
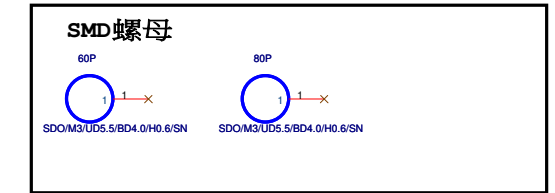
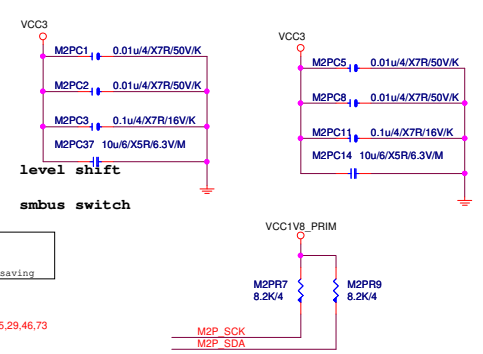
M.2 Lane2 from CPU port2

M.2 Lane1 from CPU port1



架高金屬加強

Footprint : M2_110_H2MM8W



M2P_CPU_HS

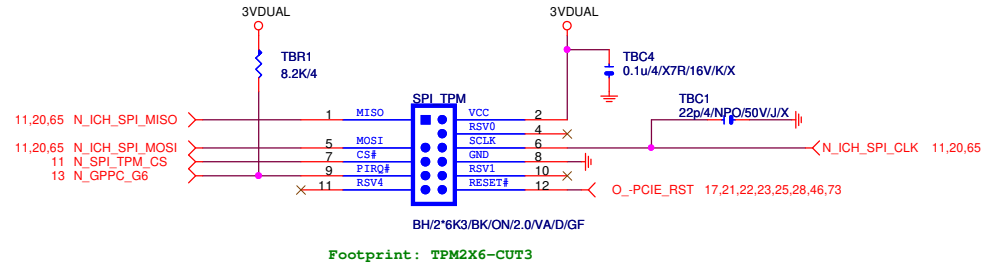
M2 HEATSINK

M2P_CPU_HS[12SP1-S13905-32R_12SP1-S13905-34R_12SP1-S13905-35R]:M2P_CPU_HS

RTD3 GPIO refer by Intel RVP

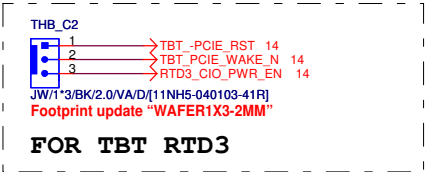
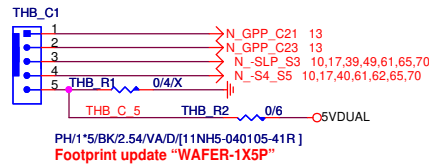
GPIO	CFL-S	CML-U	CML-H	CML-S
TBT_PERST_N	GPP_F_2	GPPC_C15_SLOT1_RST_N	GPP_F4_SATAPCIE7	GPP_F2
TBT_Wake_N	GPP_H_15	GPPC_D11_SLOT1_WAKE_N	GPPK_18	GPP_H15
RTD3_PWN_EN	GPP_I_5	GPPC_D15	GPP_H_16_SML4_CLK	GPP_K23

TPM CONNECT



Thunderbolt

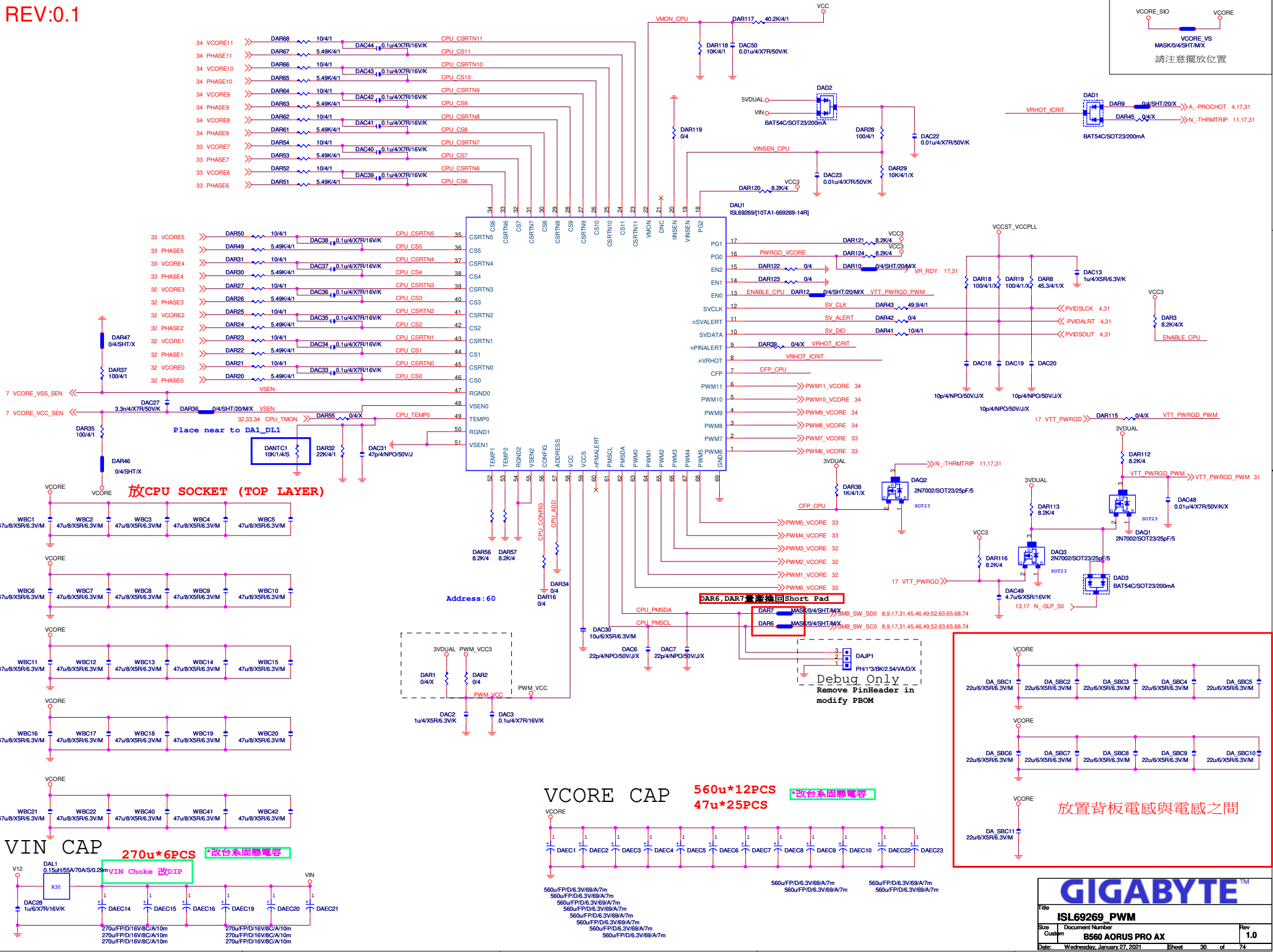
★Update 2015-12-29



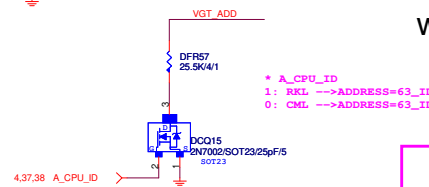
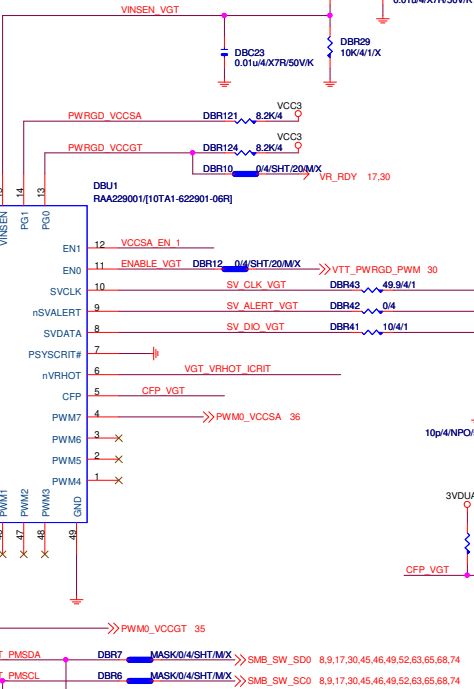
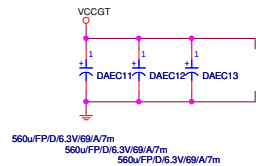
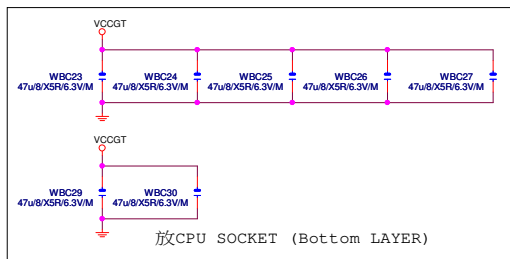
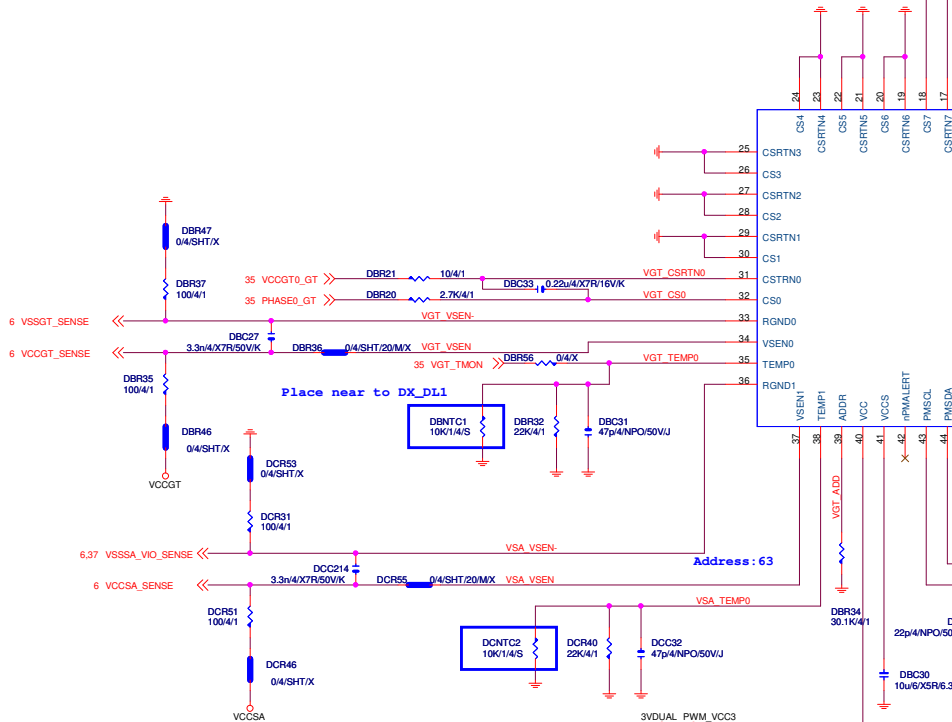
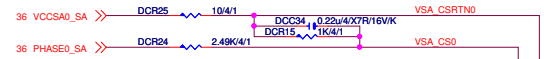
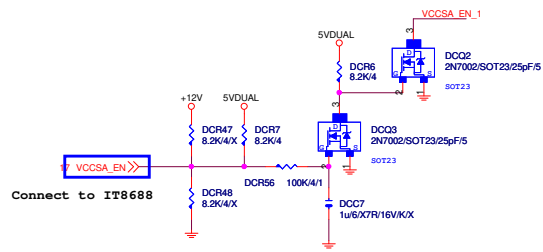
Z490系列使用

TBT_-PCIE_RST : CFL connector to GPP_F_2
TBT_PCIE_WAKE_N : CFL connector to GPP_H_15
RTD3_CIO_PWR_EN : CFL connector to GPP_K_23

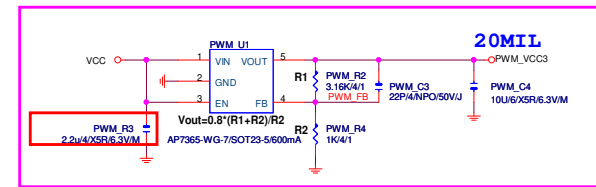
REV:0.1



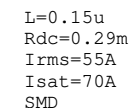
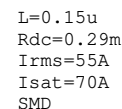
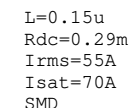
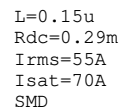
REV:0.1



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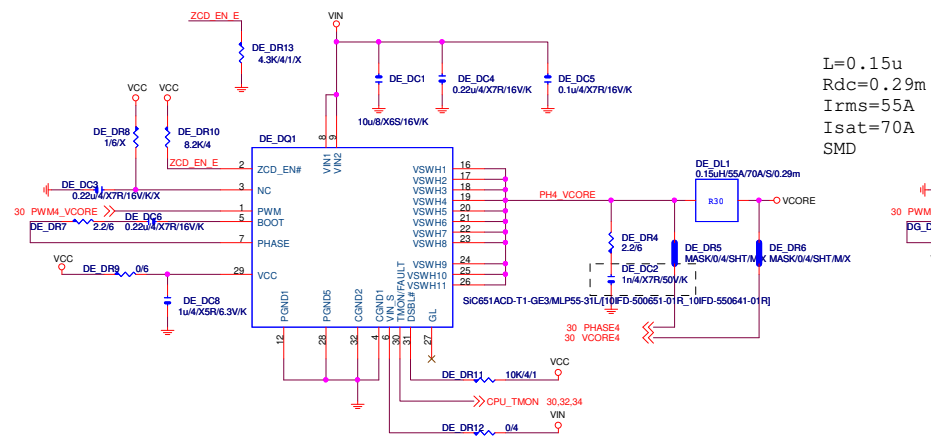


DRMOS使用NCP302155時PIN2 and PIN3要上件(Ex:DA_DR13.DA_DR8.DA_DC3)

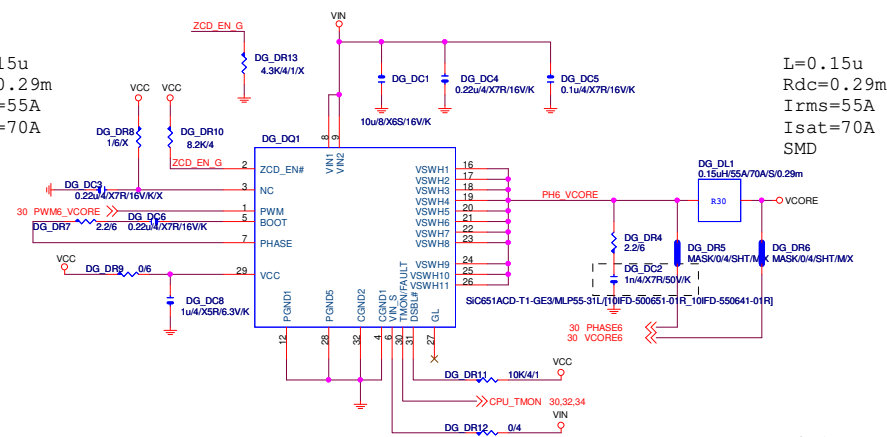


REV:0.1

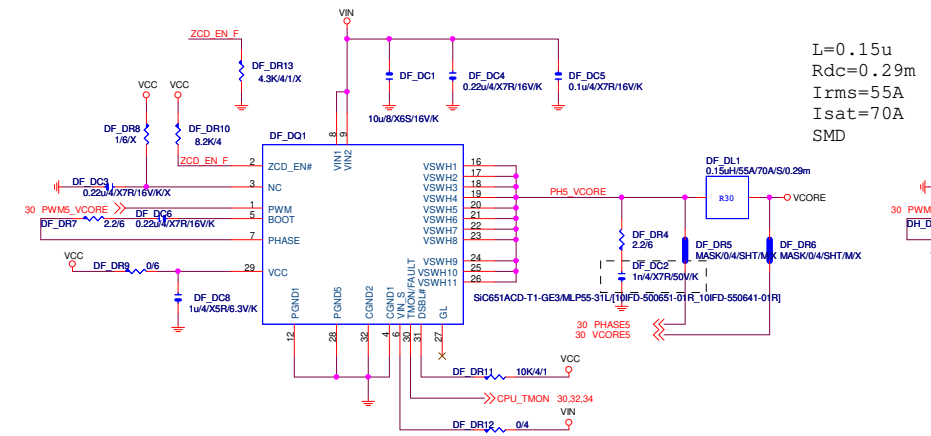
DRMOS使用NCP302155時PIN2 and PIN3要上件(Ex:DA_DR13.DA_DR8.DA_DC3)



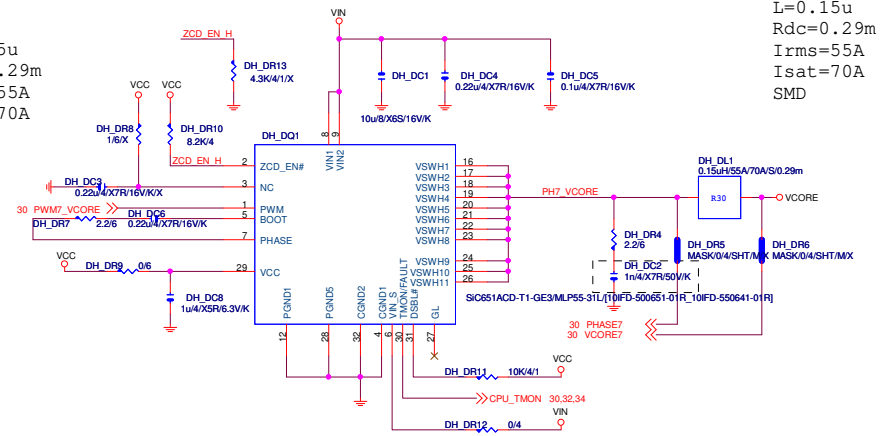
L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



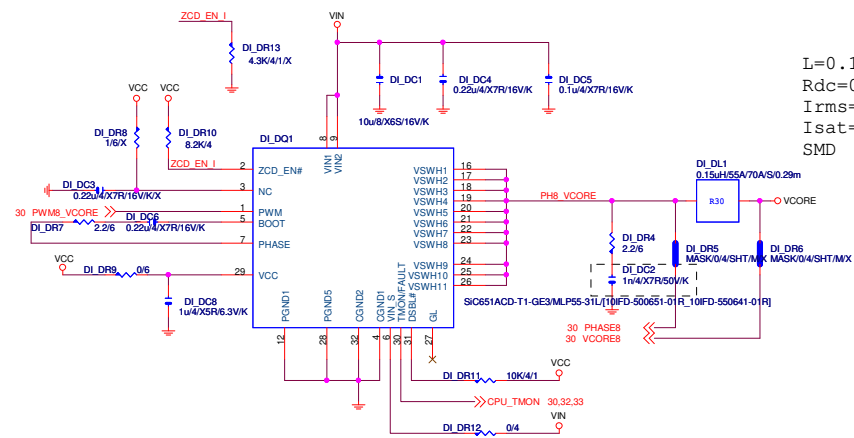
L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



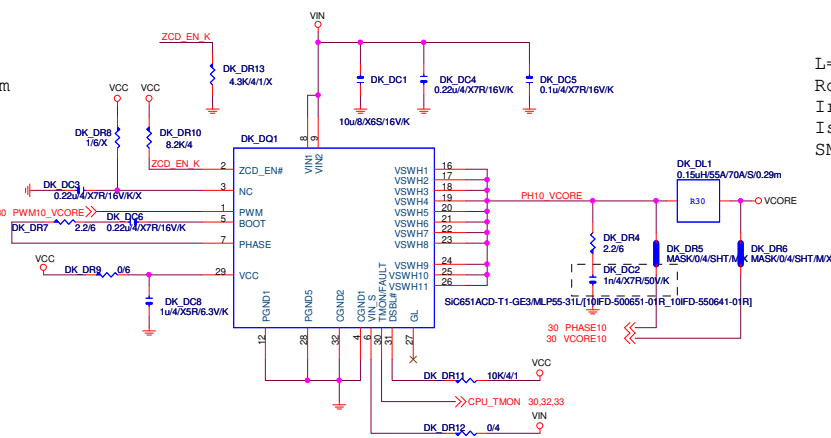
L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



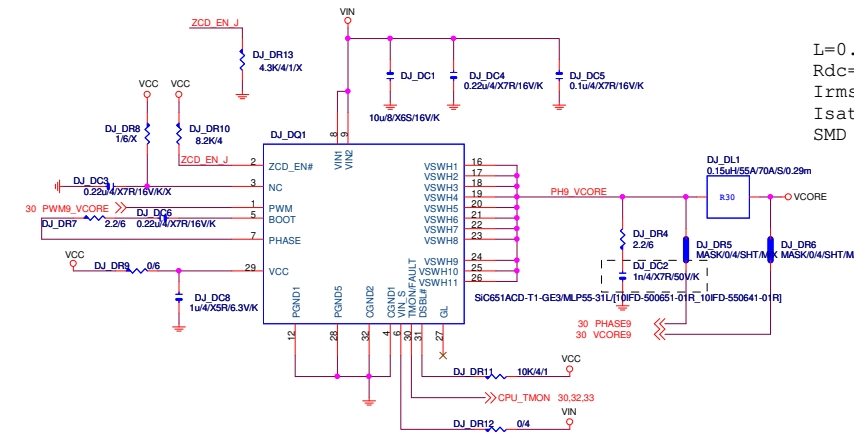
L=0.15u
Rdc=0.29m
I_{rms}=55A
I_{sat}=70A
SMD



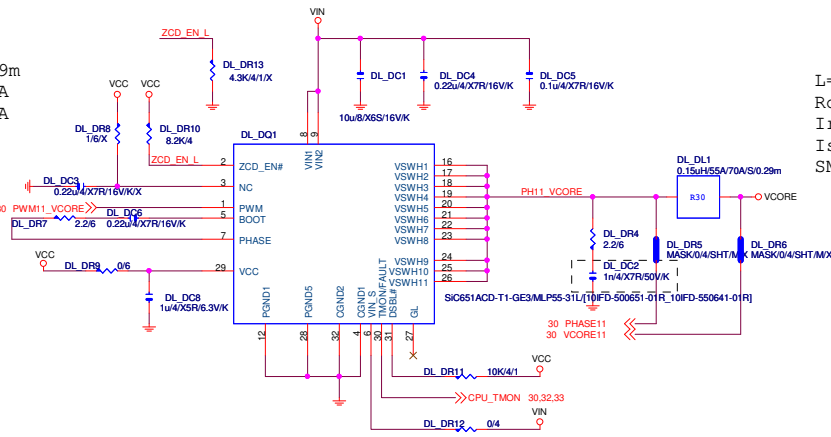
L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



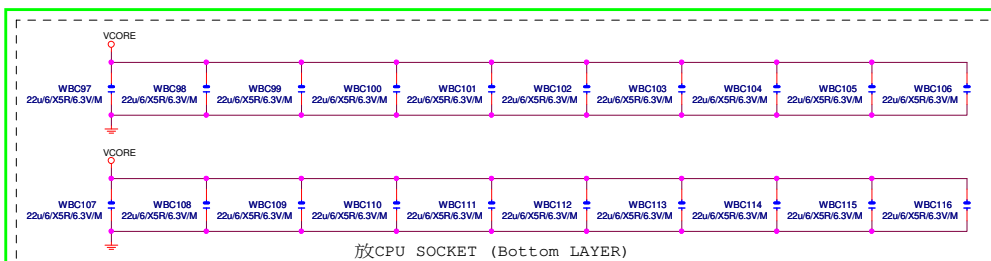
L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



L=0.15u
Rdc=0.29m
Irms=55A
Isat=70A
SMD



放CPU SOCKET (Bottom LAYER)

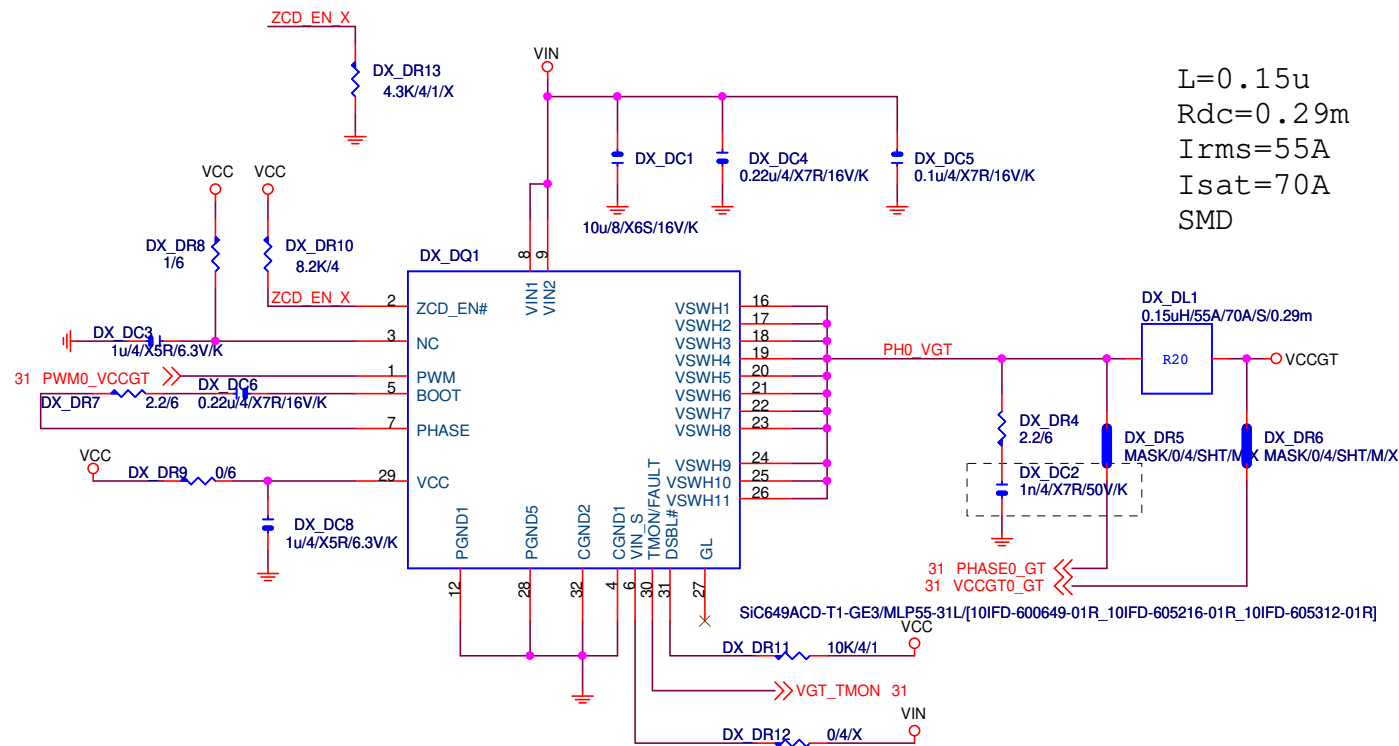
放CPU SOCKET (Bottom LAYER)

請版主自行確認是否使用
請版主自行確認使用330u or 470u

請版主自行確認使用組態

REV:0.1

DRMOS使用NCP302155時PIN2 and PIN3要上件 (Ex:DA_DR13.DA_DR8.DA_DC3)



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Title

VCCGT_DRMOS

Size
Custom

Document Number

B560 AORUS PRO AX

Rev

1.0

Date:

Wednesday, January 27, 2021

Sheet

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of

74

$L=0.33\mu$
 $R_{dc}=2.4m$
 $I_{rms}=23A$
 $I_{sat}=25A$

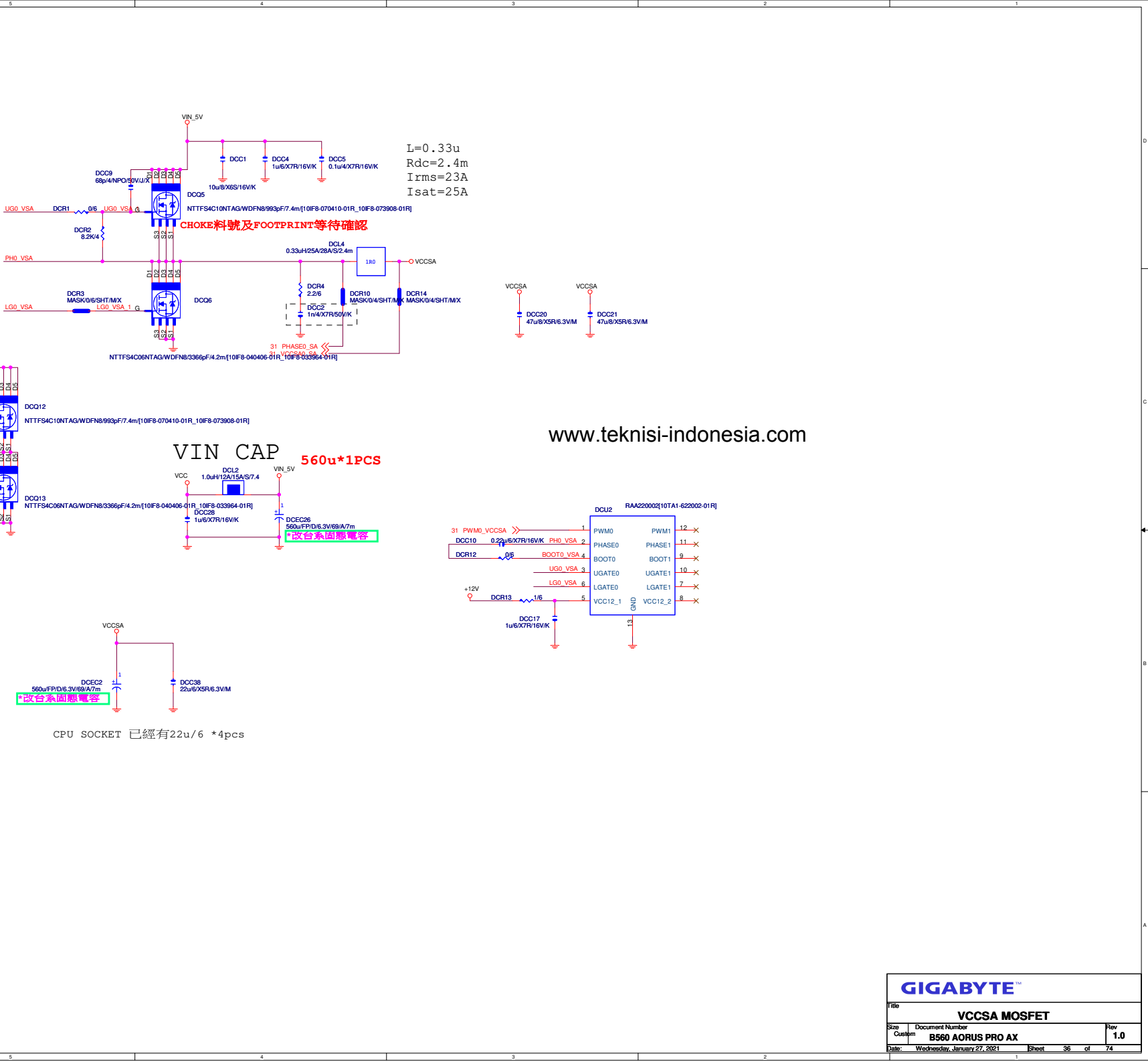
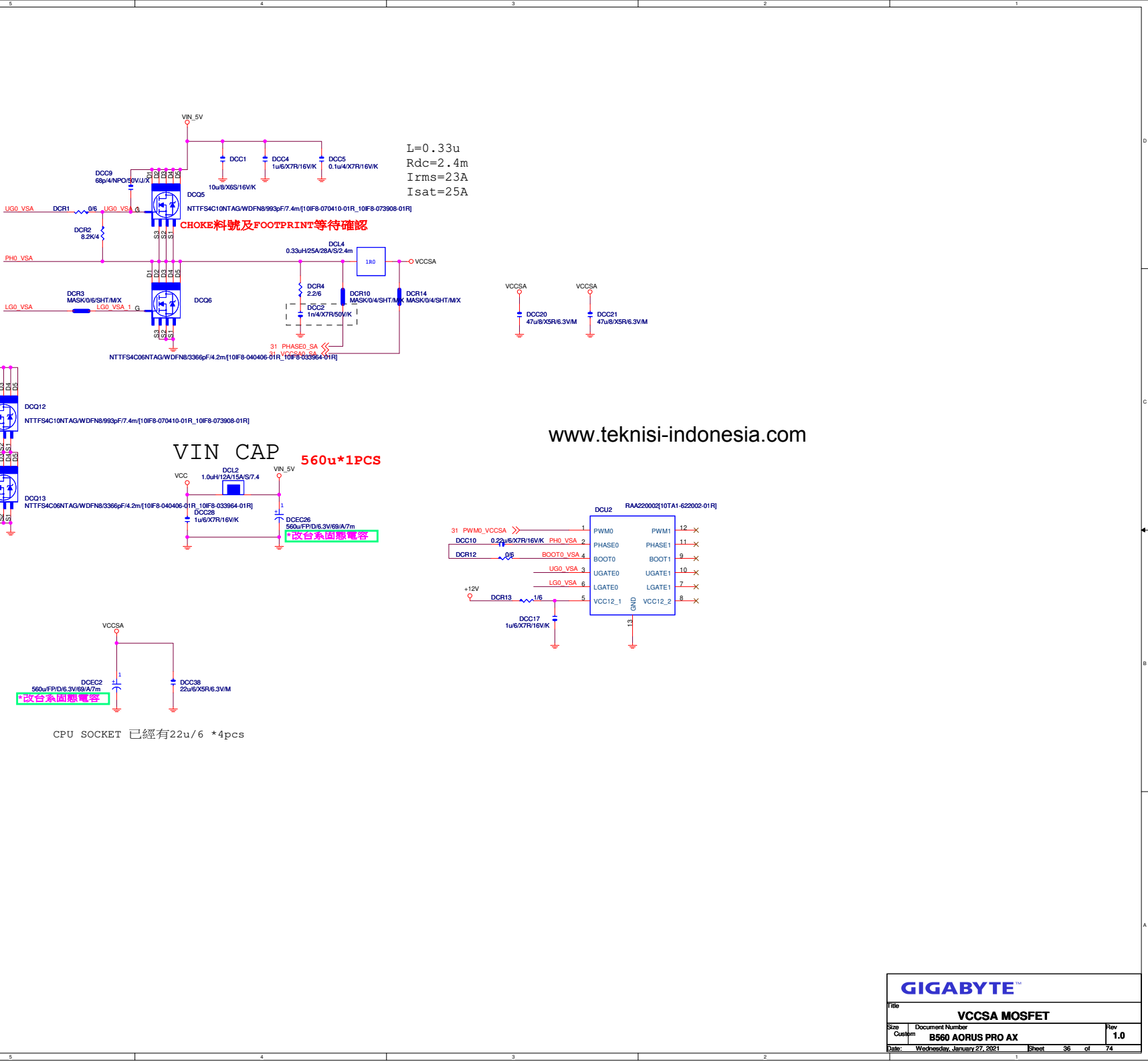
CHOKER料號及FOOTPRINT等待確認

VIN CAP 560u*1PCS

CPU SOCKET 已經有22u/6 * 4pcs

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 B560 AORUS PRO AX
 VCCSA MOSFET
 Date: Wednesday, January 27, 2021 Sheet 36 of 74



$L=0.33\mu$
 $R_{dc}=2.4m$
 $I_{rms}=23A$
 $I_{sat}=25A$

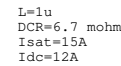
CHOKER料號及FOOTPRINT等待確認

VIN CAP 560u*1PCS

CPU SOCKET 已經有22u/6 * 4pcs

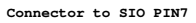
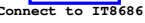
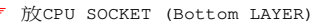
www.teknisi-indonesia.com

GIGABYTE™
 B560 AORUS PRO AX
 VCCSA MOSFET
 Date: Wednesday, January 27, 2021 Sheet 36 of 74

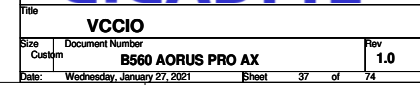


CHOKES與CAP料號可變

注意耐壓



Mode	VR	Mode logic	LPM	VID Setting		Vout (V)
				G1 logic	G0 logic	
Mode1	VCCIO	0	0	x	x	0(LPM)
			1	0	0	0.85
			1	0	1	0.875
			1	1	0	0.95
			1	1	1	0.975
			0	x	x	0.7V(LPM)
Mode2	VPRIMCORE	Floating	1	0	0	0.85
			1	0	1	0.9
			1	1	0	0.95
			1	1	1	1
			0	x	x	0(LPM)
			1	0	0	0.8
Mode3	VccEDRAM/ VccEOPIO	1	1	0	1	0.95
			1	1	0	1
			1	1	1	1.05
			0	x	x	0(LPM)
			1	0	0	0.8
			1	0	1	0.95



VCCIO2

REV: 0.1

RKL MODIFY

VCC3

DGR25

VCCIO2_PG

VCCIO2_EN_1

VCC1V8_P1M

VIO2_LPM

VCCIO2_PG

VCCIO2_EN_1

VCCIO2_CS

VCCIO2_MODE

VCCIO2_G0

VCCIO2_G1

VCCIO2_G1

VCCIO2_G0

VCCIO2_MODE

VCCIO2_G1

VCCIO2_G0

VCCIO2_MODE

VCCIO2_G1

VCCIO2_G0

VCCIO2_MODE

VCCIO2_G1

VCCIO2_G0

VCCIO2_MODE

VCCIO2_G1

VCCIO2_G0

VCCIO2_MODE

VCCIO2_G1

VCCIO2_G0

有使用CPU POWER時DCR22不上件

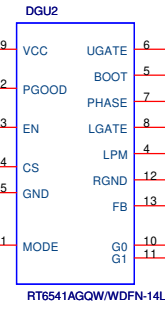
Connect to IT8795

Connect to IT8686

Connect to PCH

* CPU_ID
1: RKL -->VCCIO=0.95V
0: CML -->VCCIO=0V

4,31,37 A_CPU_ID



VCCIO2_EN_1

5VDUAL

DGR21

DGR22

DGR23

DGC16

DGR37

MASK0/4/SHT/X

DGR38

DGR39

DGR40

DGR41

DGR42

DGR14

DGR15

DGR16

DGR17

DGR18

DGR19

DGR20

DGR24

DGR25

DGR26

DGR21

DGR22

DGR23

DGC16

DGR37

MASK0/4/SHT/X

DGR38

DGR39

DGR40

DGR41

DGR42

DGR14

DGR15

DGR16

DGR17

DGR18

DGR19

DGR20

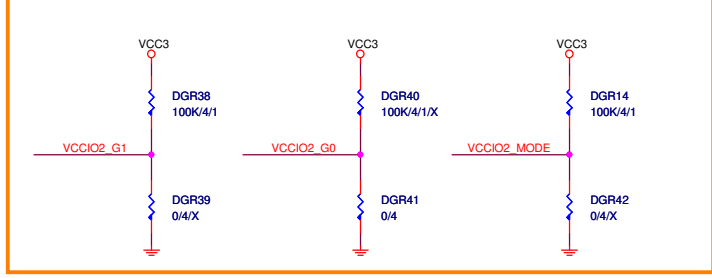
DGR24

DGR25

DGR26

DGR27

DGR28



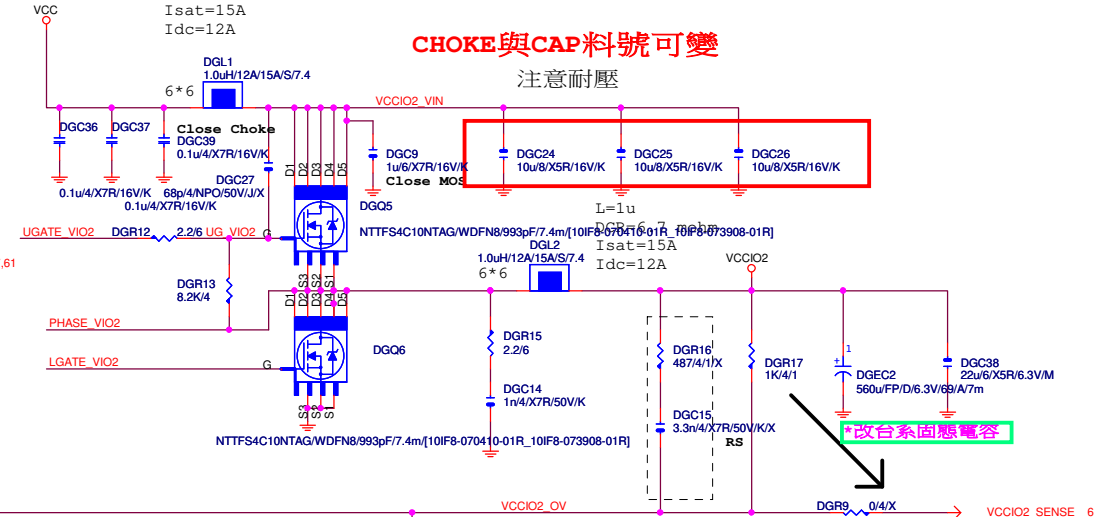
從output CAP端拉回

ADDRESS=24 63 VCCIO2_OV
VREF=02

L=1u
DCR=6.7 mohm
Isat=15A
Idc=12A

CHOKE與CAP料號可變

注意耐壓



Remote sense請從最重的負載端點拉回

*改台系固態電容

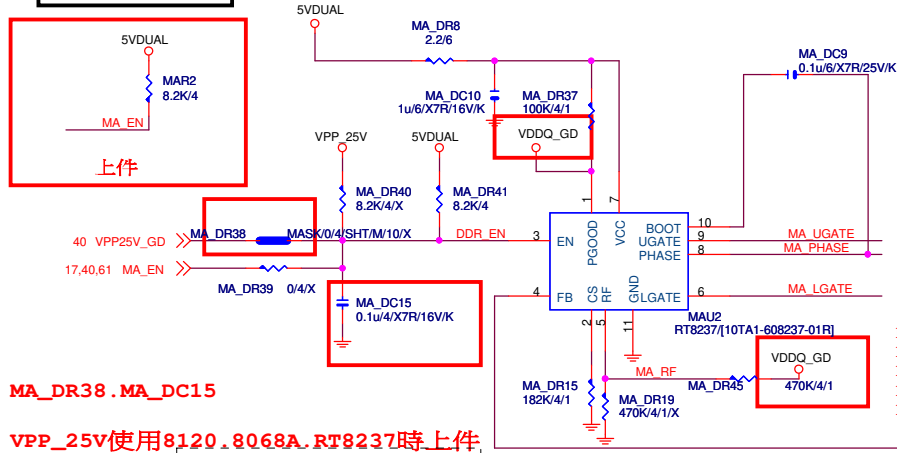
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VCCIO2

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REV: 0.11

DDR4



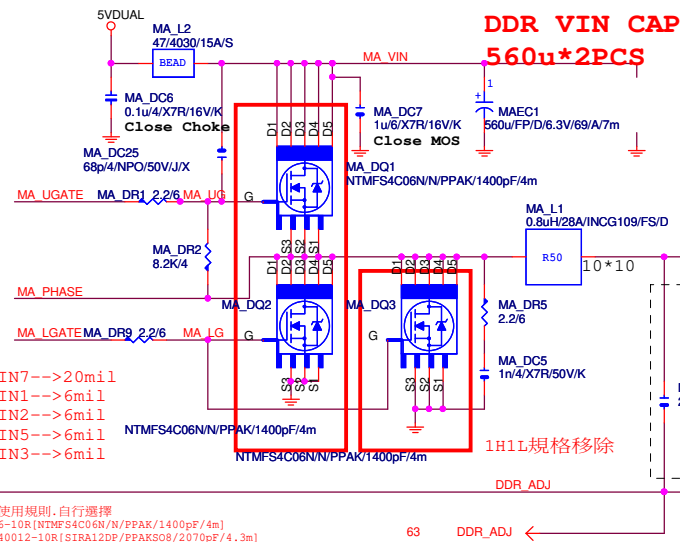
MA_DR38.MA_DC15

VPP_25V使用8120.8068A.RT8237時上件

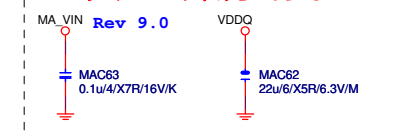


FS=290K
OCP=40A

MOSFET請依MOSFET使用規則,自行選擇
ON-->10IF9-040406-10R[NTMFS4C06N/N/PPAK/1400pF/4m]
VISHAY-->10IF9-040012-10R[SIRA12DP/PPAKS08/2070pF/4.3m]



CHOKE與CAP料號可變



SUPPORT DDR4 1.2V

25A MAX

L=1u
DCR=2.5 mohm
Isat=35A
Idc=28A

請放置CHOKE一出來位置.先預留.
請自行確認ripple後再決定是否上件

Remote sense請從最重的負載端點拉回

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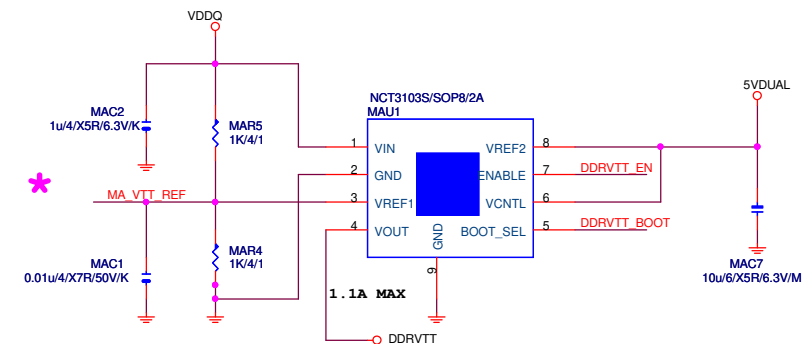
PWR SEQ

CLOSE TO DDR POWER PLANE

For power sequence require

VPP_25V使用8120時上件

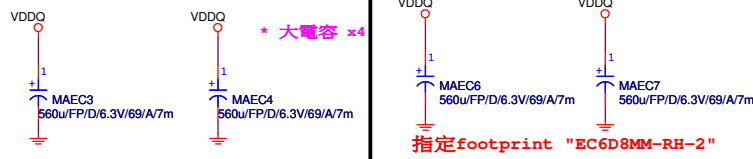
MAU1上RT9045時上件(不可MASK)

DDRVTT

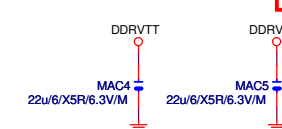
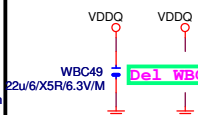
DDR_VTT_CTL	MAR110	MASK/0/4/SHT/M/10/X	DDRVTT_EN
N_SLP_S3	MAR111	MASK/0/4/SHT/M/10/X	DDRVTT_BOOT


DDRVTT CAP

* 大電容 x0



指定footprint "EC6D8MM-RH-2"

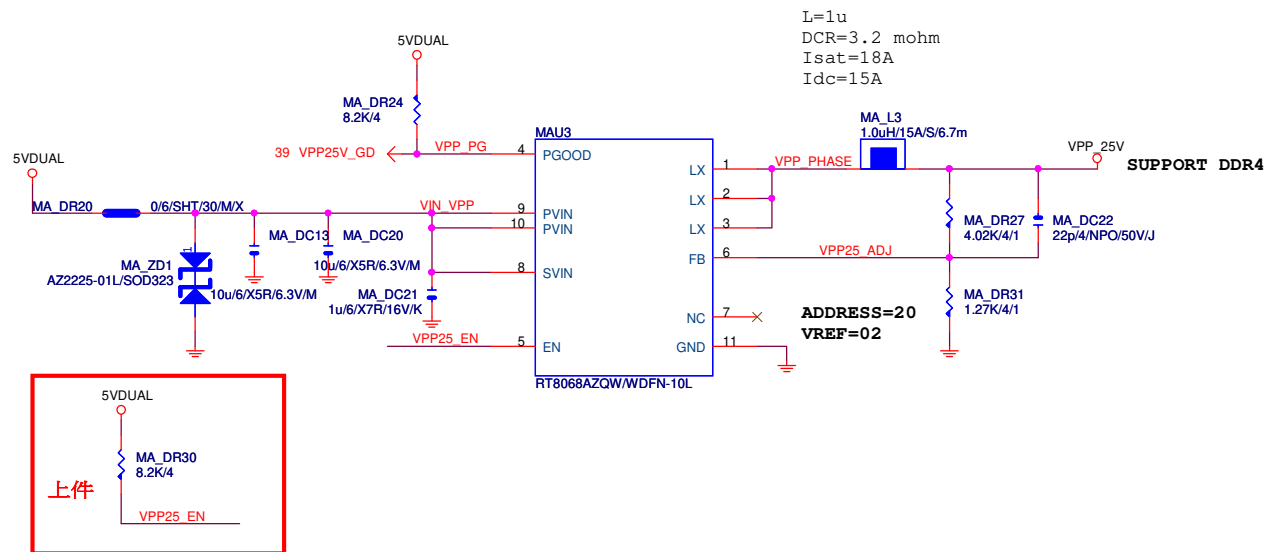


			
Title RT8237 DDR4 POWER			
Size Custom	Document Number B560 AORUS PRO AX		Rev 1.0
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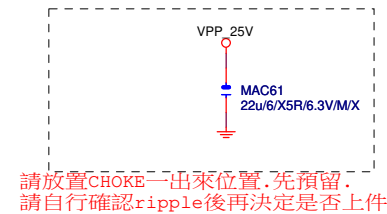
REV:0.1

VPP 25V

CHOKE與CAP料號可變

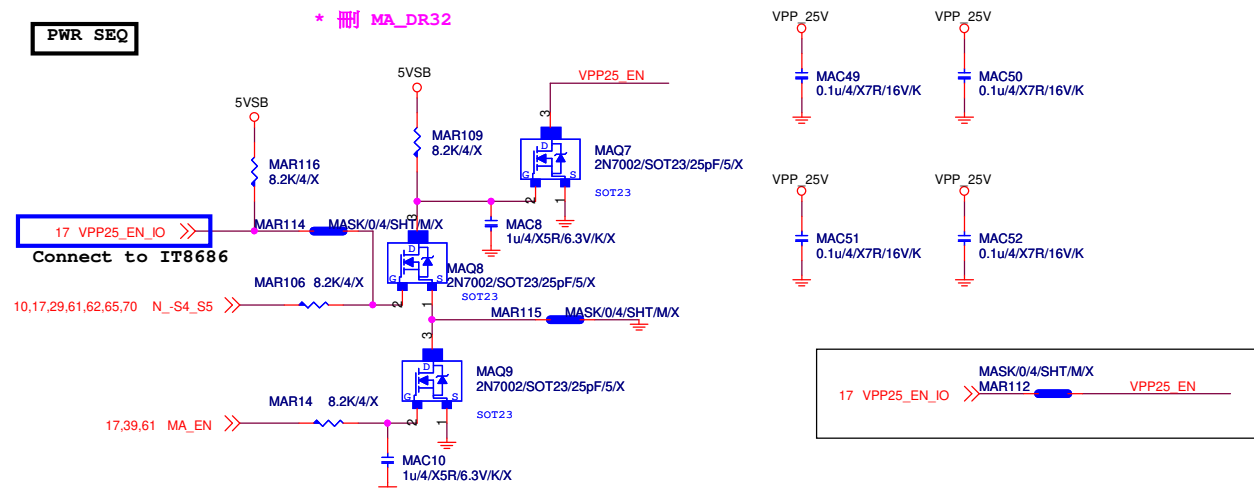


2.5V

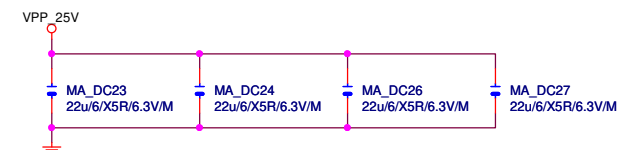


PWR SEQ

* 刪 MA_DR32

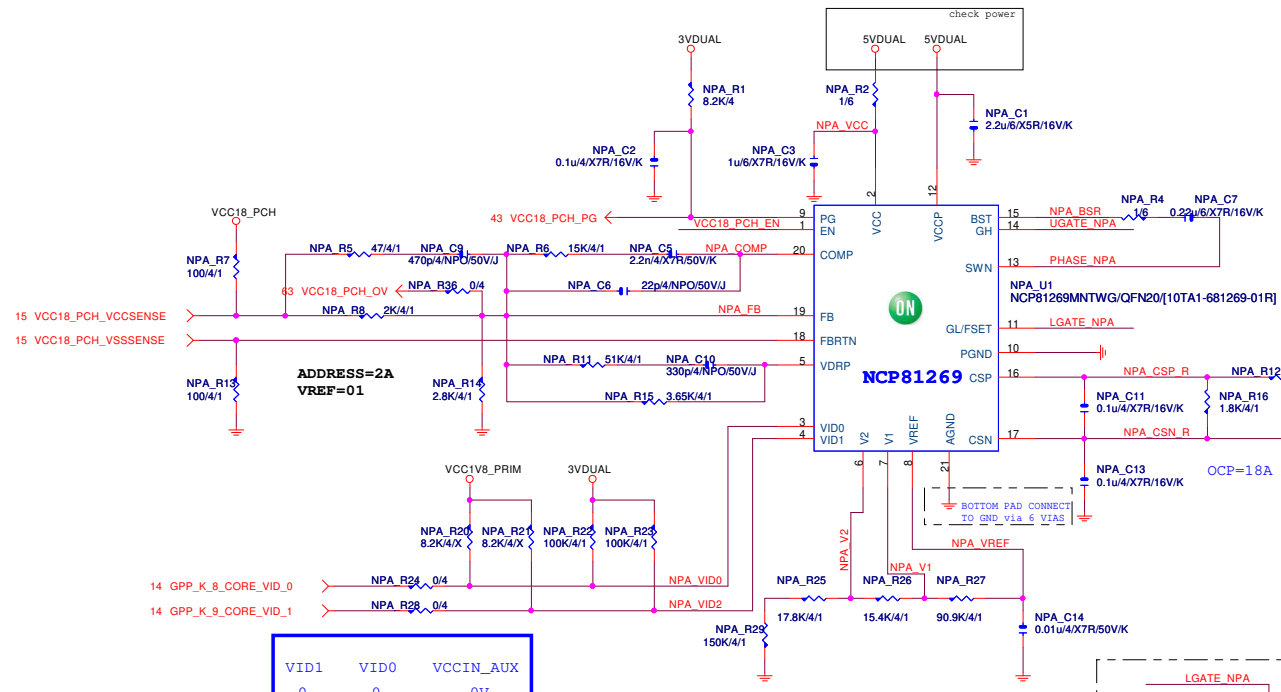


VPP CAP 22u*4PCS

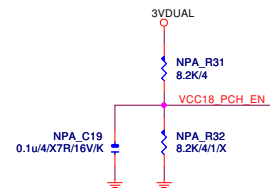


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Title		
RT8068_VPP25 POWER		
Size	Document Number	Rev
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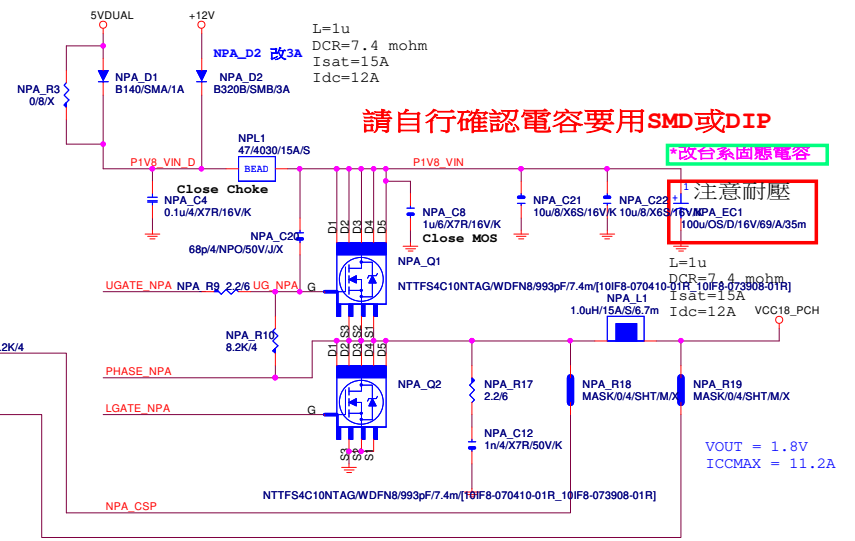


VID1	VID0	VCCIN_AUX
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

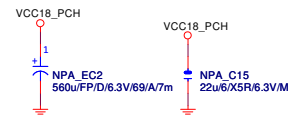


connect to SIO 17 VCC1_0_EN NPA_R33 0/4/X VCC18_PCH_EN
 connect to VCC1V8_PRIM GD 42 VCC1V8P_GD NPA_R34 0/4 VCC18_PCH_EN
 connect to PCH pin AD46 11,42 SLP_SUS_N NPA_R35 0/4/X VCC18_PCH_EN

VCC18_PCH_EN 線路



請自行確認電容要用SMD或DIP

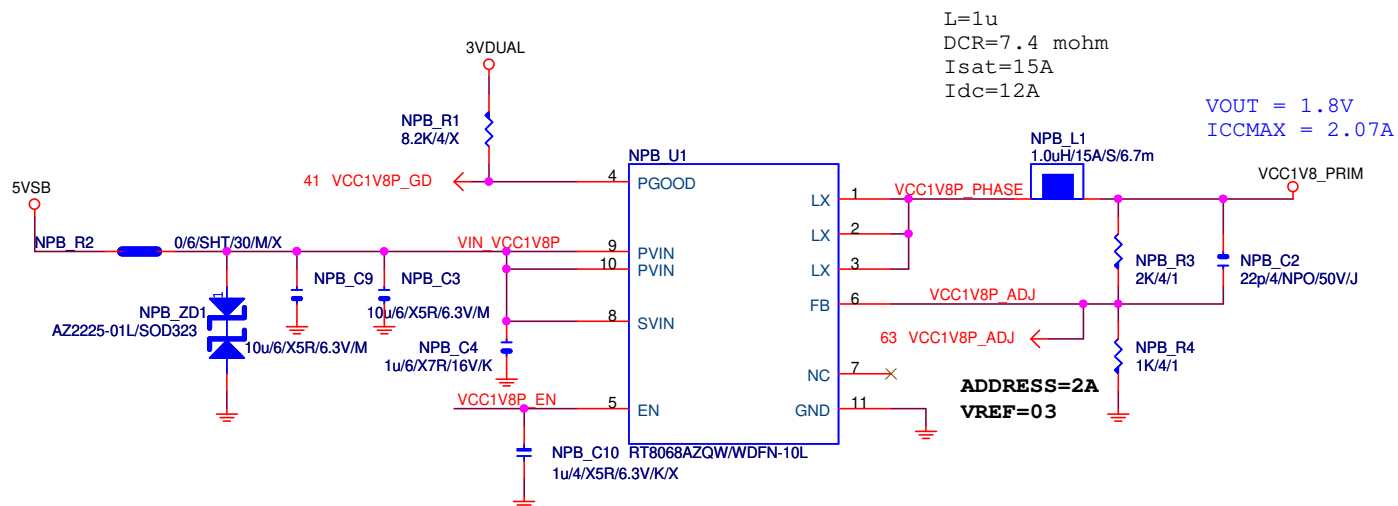


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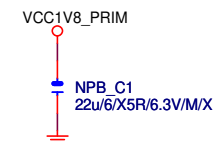
Title	NCP81269_PCH POWER		
Size	Document Number	Rev	
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REV:0.1

VCC1V8 PRIM

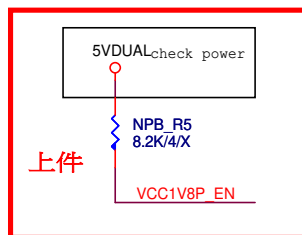


CHOKE與CAP料號可變



請放置CHOKE一出來位置.先預留.
請自行確認ripple後再決定是否上件

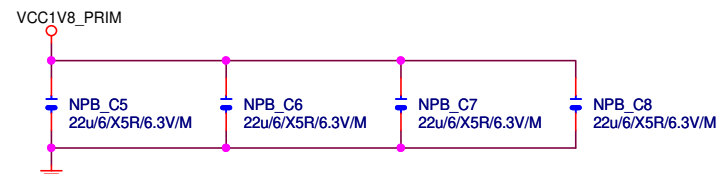
PWR SEQ



connect to PCH pin AD46



VCC1V8_PRIM CAP 22u*4PCS



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Title
RT8068_VCC1V8_PRIM

Size Document Number
Custom B560 AORUS PRO AX

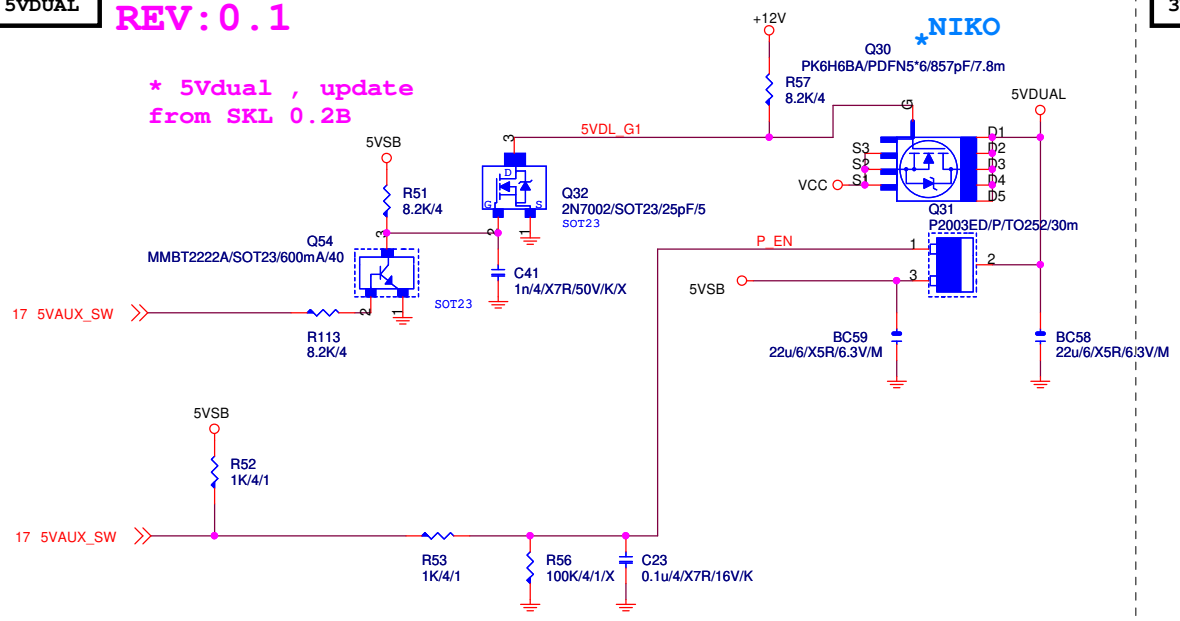
Rev
1.0

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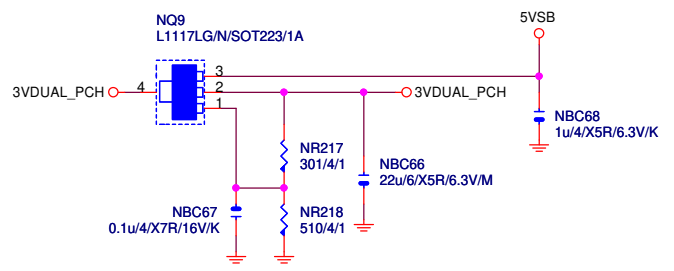
5VDUAL

REV:0.1

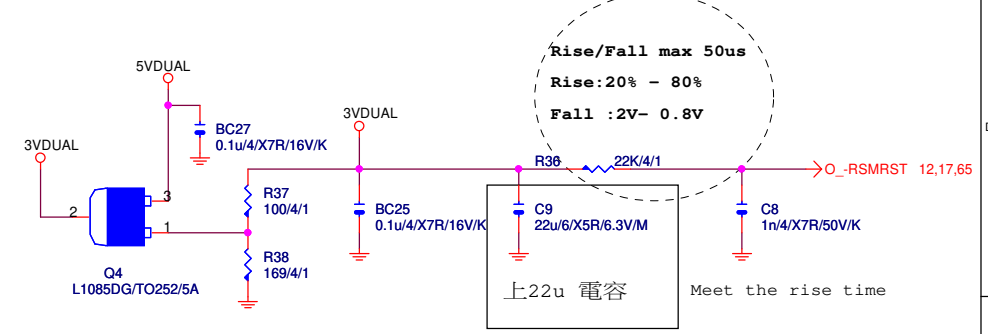
* 5Vdual , update
from SKL 0.2B



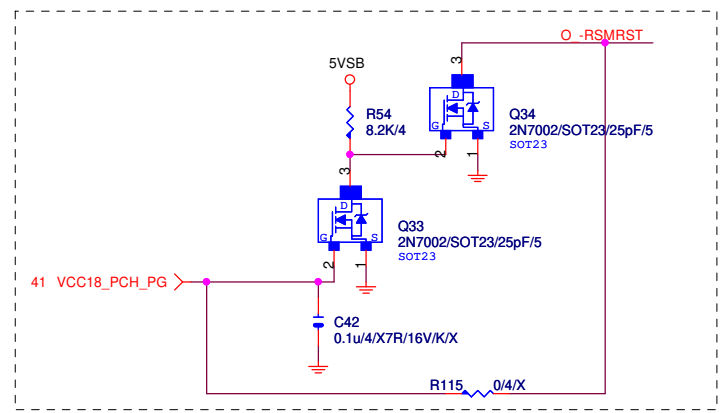
3VDUAL_PCH



3VDUAL

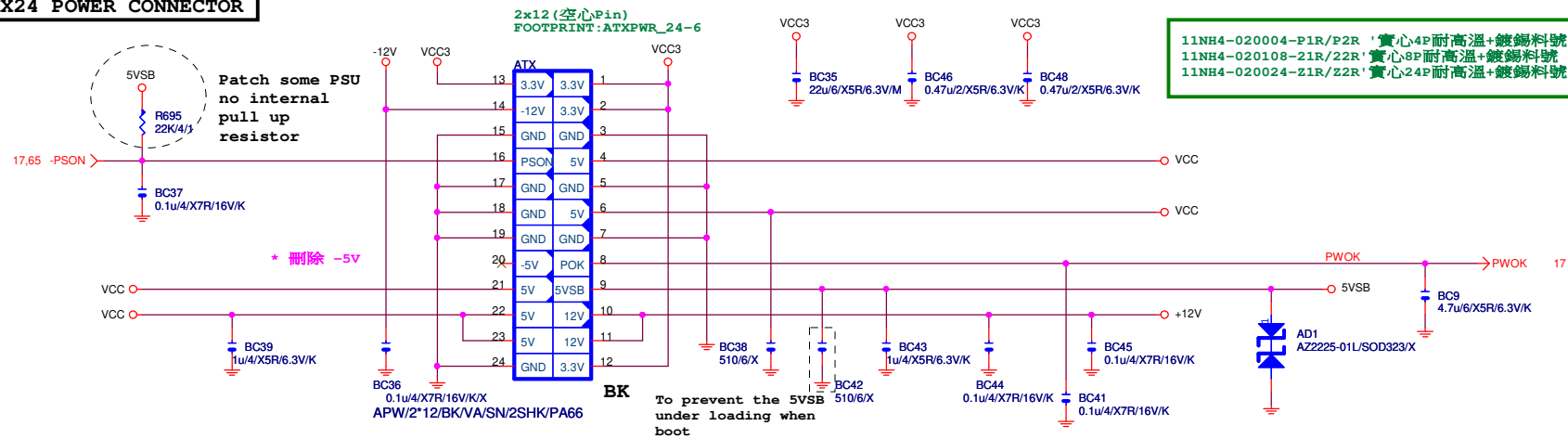


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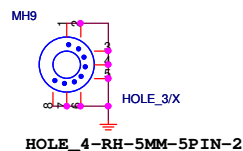
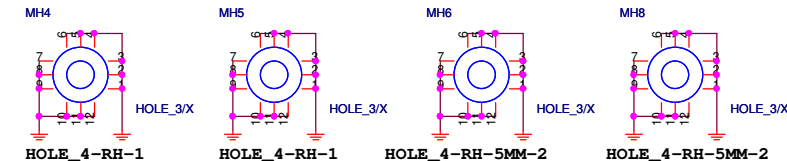
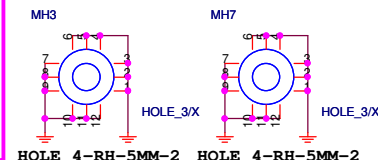
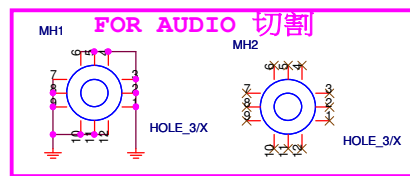
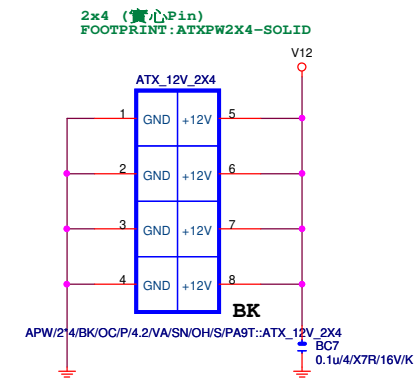


Gigabyte Technology			
Title			
DISCRETE POWER			
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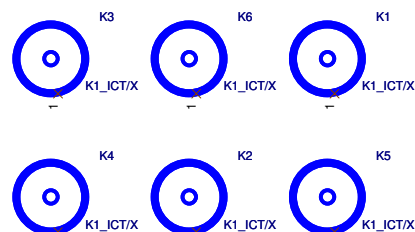
ATXX24 POWER CONNECTOR



ATXX4 POWER CONNECTOR

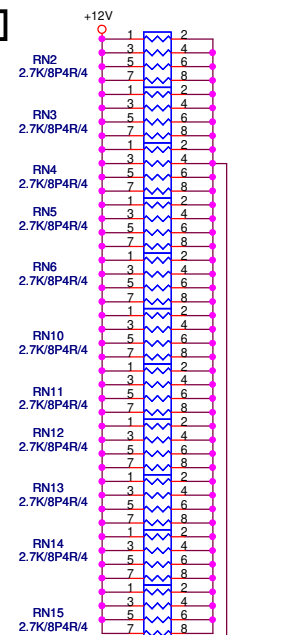


固定孔/光學點

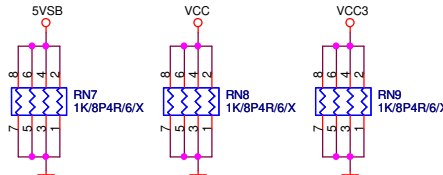


+12V DUMMY LOAD

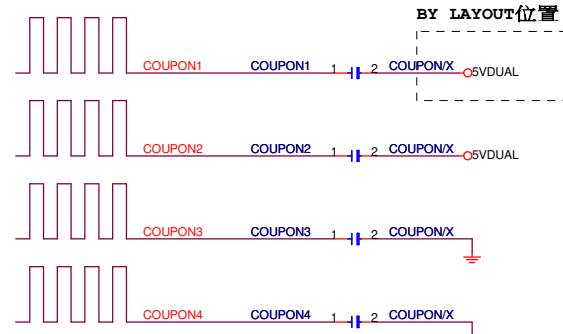
To fix 12V light load
abnromal issue



DUMMY LOAD



COUPON



Gigabyte Technology

Title
ATX POWER CONNECTOR

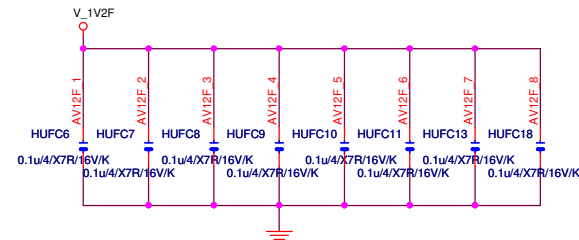
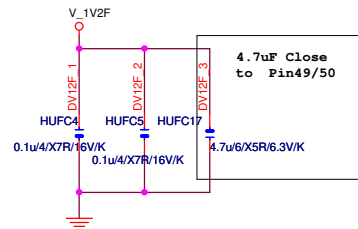
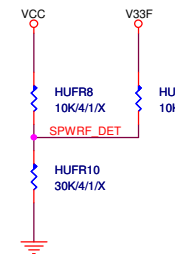
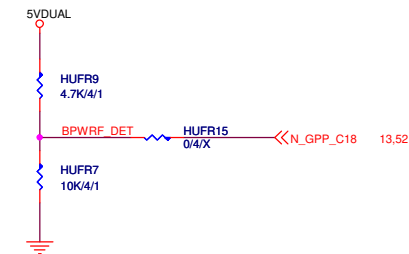
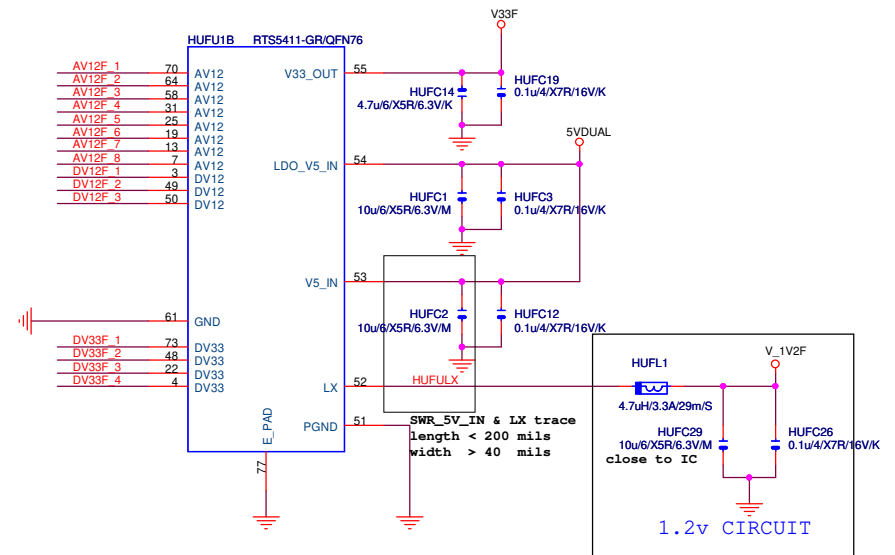
Size Custom Document Number

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B560 AORUS PRO AX

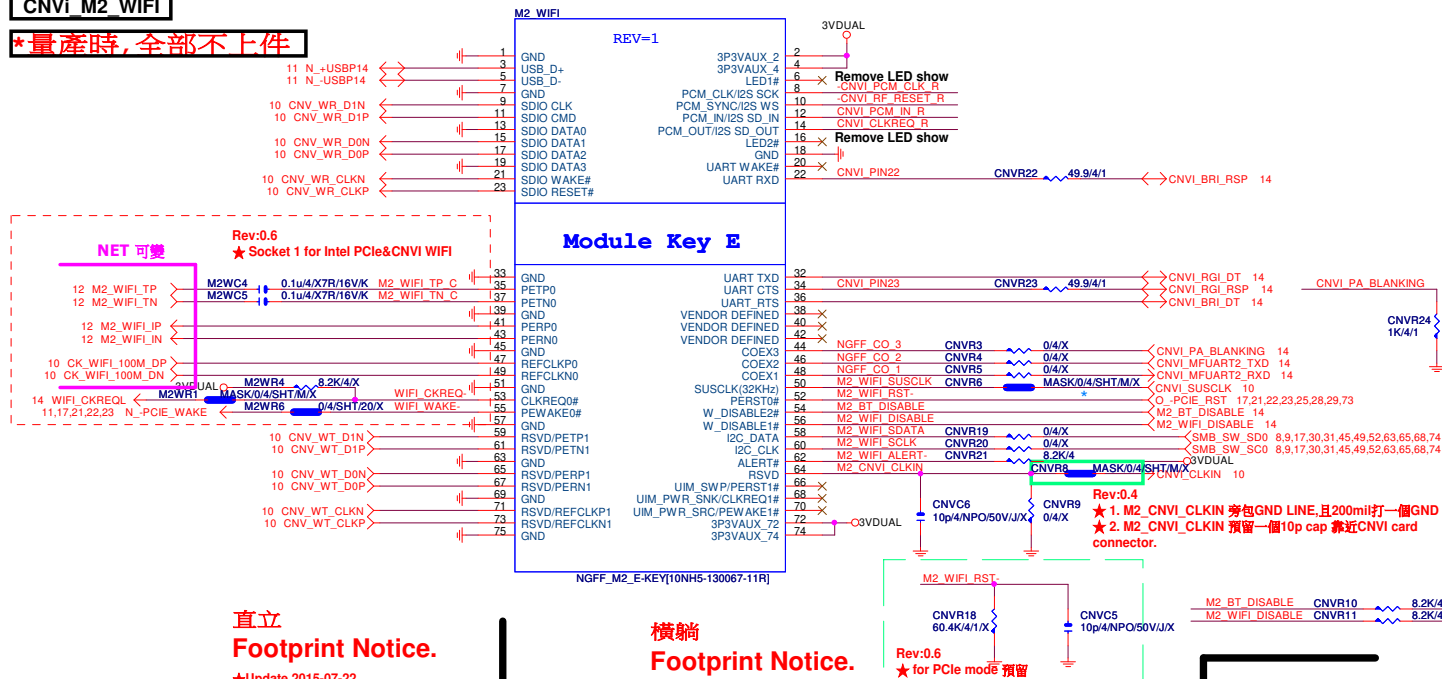
Rev 1.0

GROUP F



CNVi_M2_WIFI

支援PCIE介面WIFI及USB介面BT



直立
Footprint Notice.

★Update 2015-07-22

★Footprint for 直立式 SMD:
WIFI-EKEY

★SMD P/N: 直立式
10NH5-130067-11R.

橫躺

Footprint Notice.

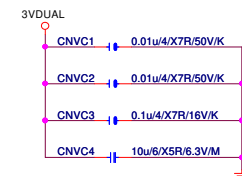
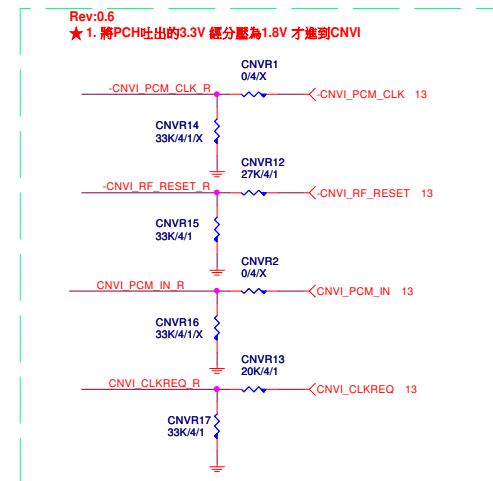
★Update 2015-07-22

★Footprint for 横躺式高:
NGFF-E-75P-3

★Footprint for 横躺式矮:
CNVI

★ 横躺式高SMD
P/N:10NR5-130067-61R

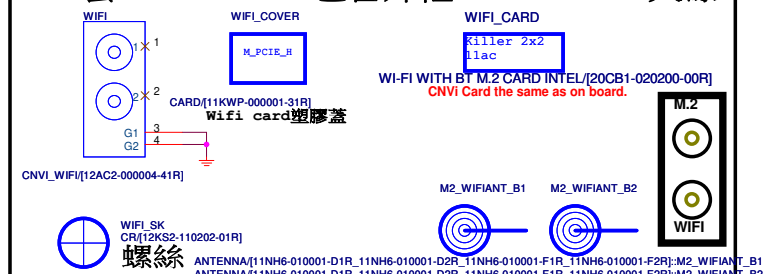
★ 横躺式矮SMD
P/N:10NR5-130067-22R



FOR M.2 WIFI MODULE @ REAR PANEL

★Update 2015-02-11

一套WIFI MODULE包含外框+WIFI CARD+天線

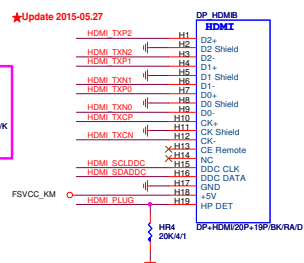
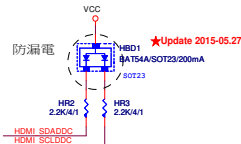


兩片式WIFI金屬殼改為單件式
Layout Library : wifi-ekey-module-1
Tiptop P/N : 12AC2-000004-31R

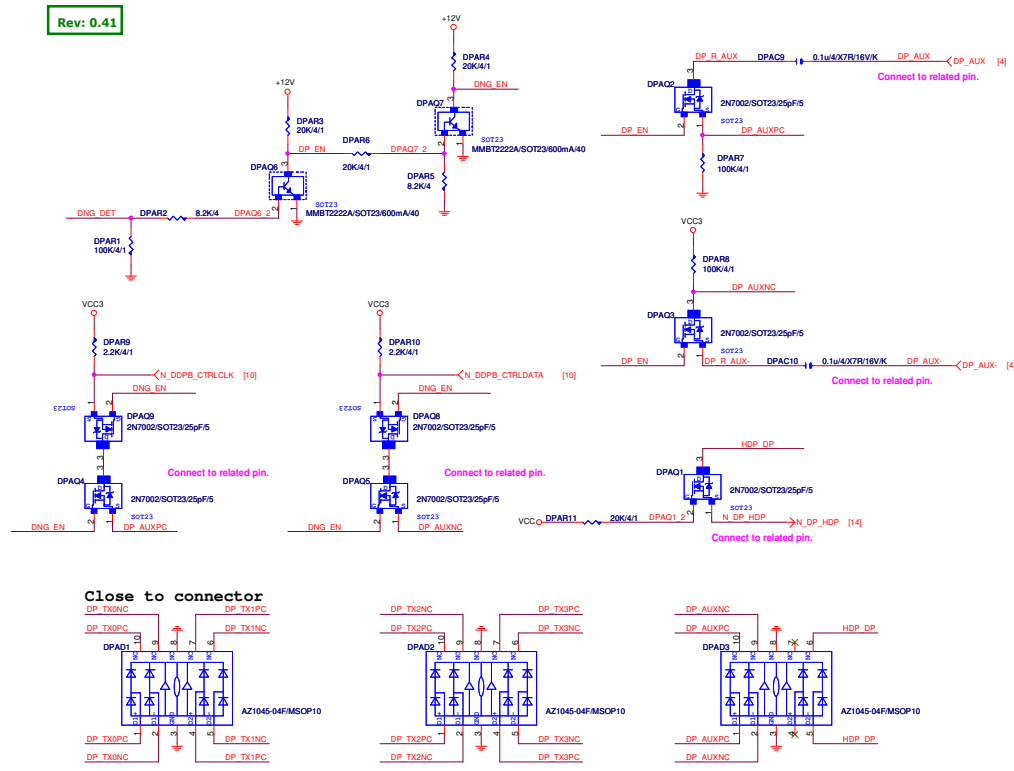
GIGABYTE™

Title			
CNVI_M2_WIFI			
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Rev: 0.81	HDMI LEVEL SHIFT
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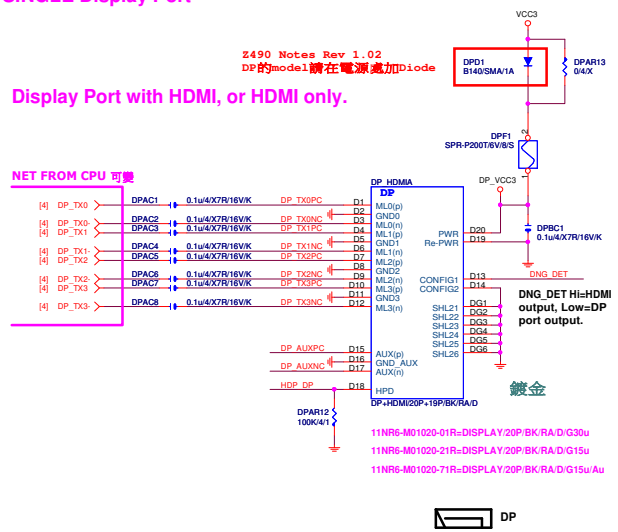


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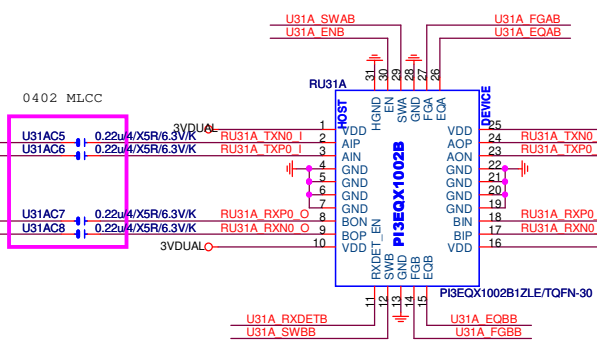
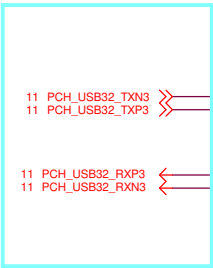


SINGLE Display Port

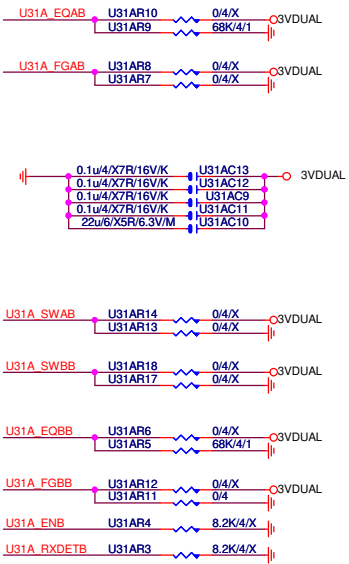
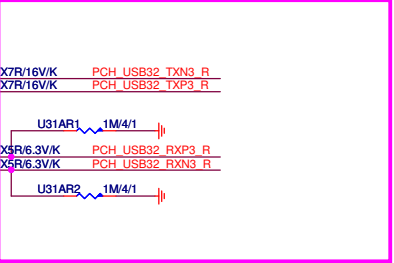
Display Port with HDMI, or HDMI only.



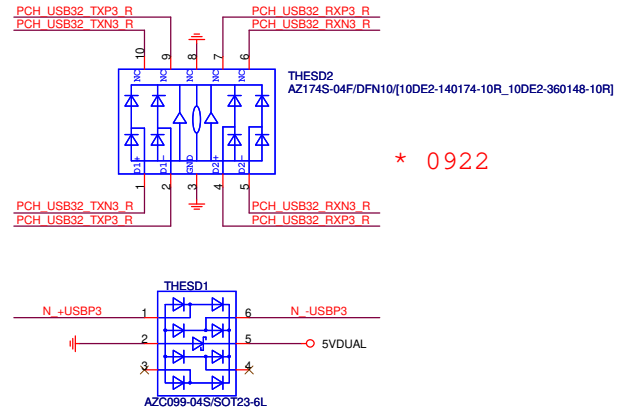
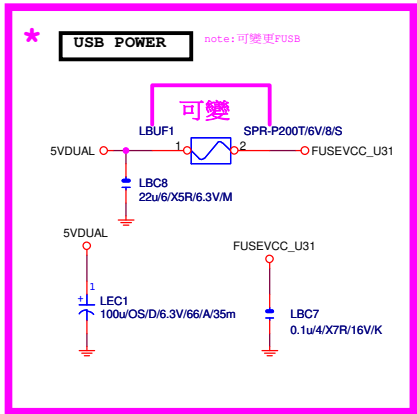
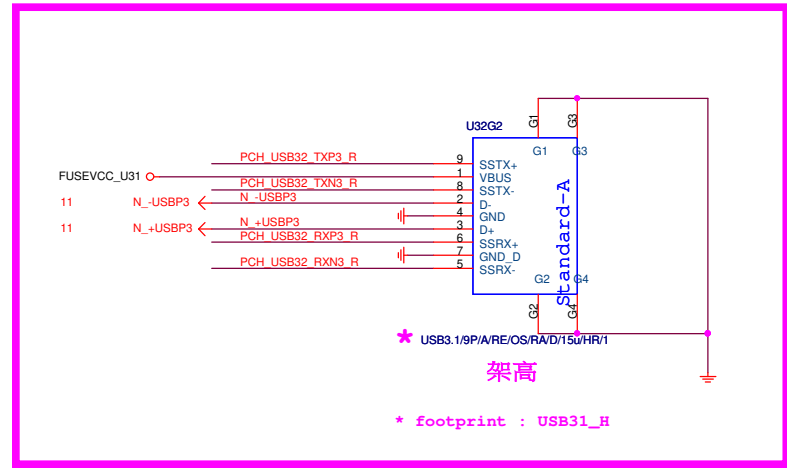
PCH Site



USB Type-A Connector Site

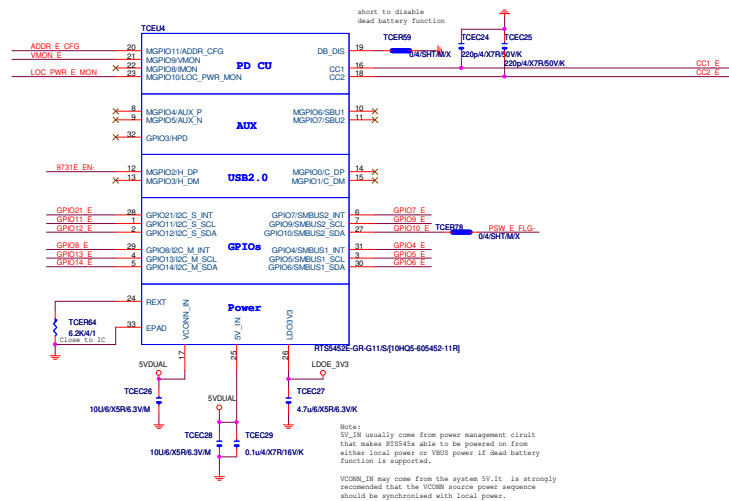
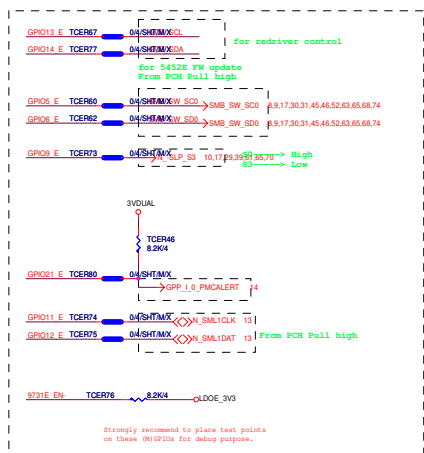
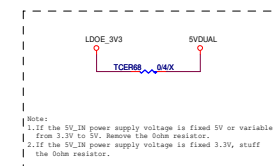
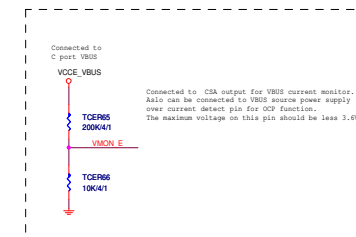
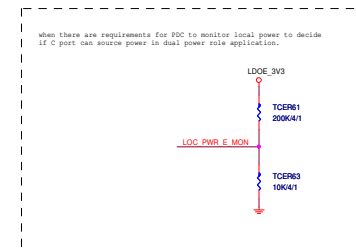
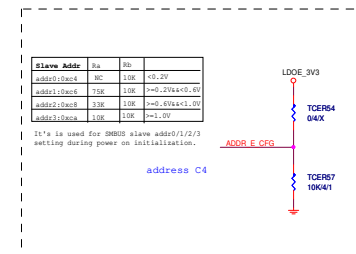
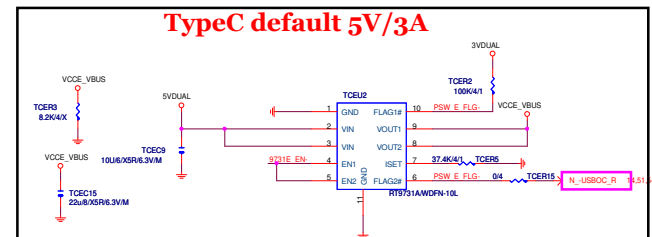
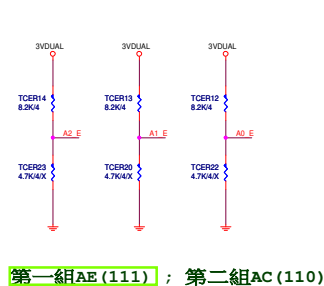
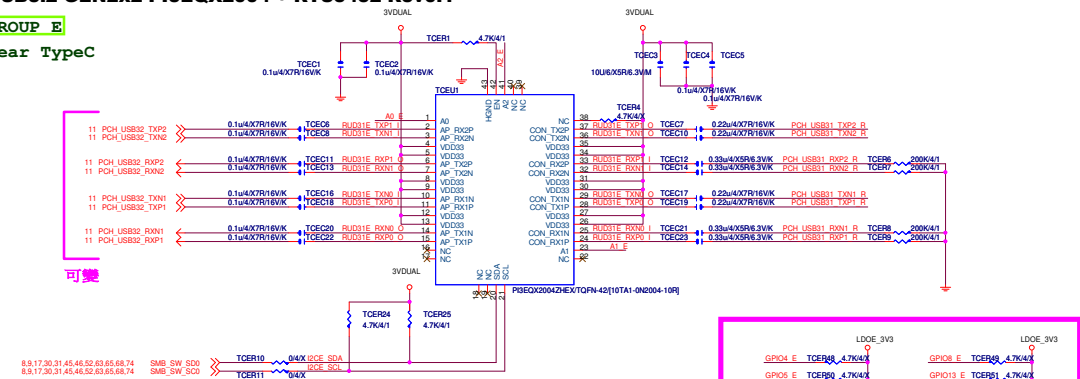


USB31 TYPE A Connector / power source / FUSE which choose for project demand

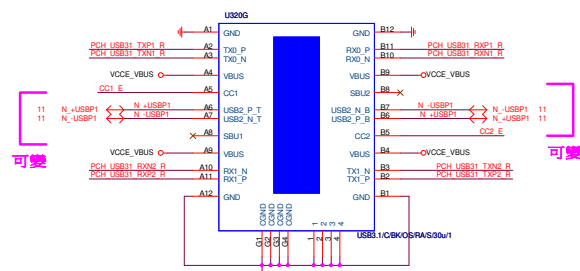


P/N SWAP

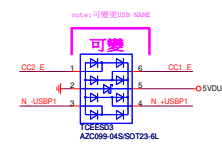
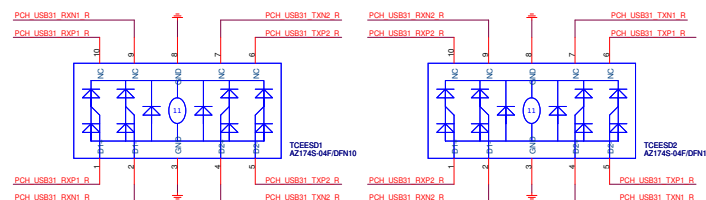
Rear TypeC



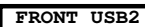
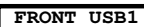
Color markers can be changed by model



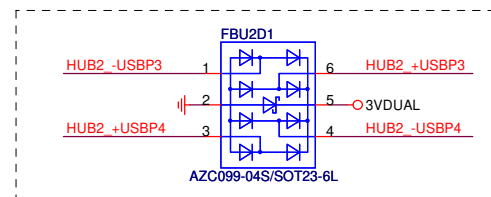
USB2.0 can be used the same source



HUB PWR



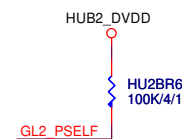
12M/20p/30ppm/3.2*2.5/80/S/10XT5-812000-40R, 10XT5-V12000-00R



Close to connector
FUSE 2 Port 1 Fuse 2A



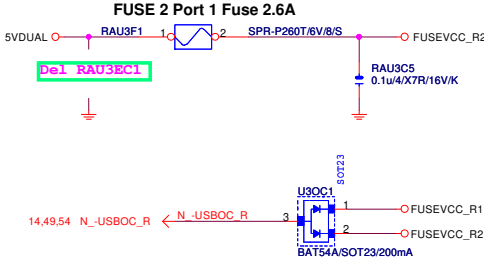
PSELF



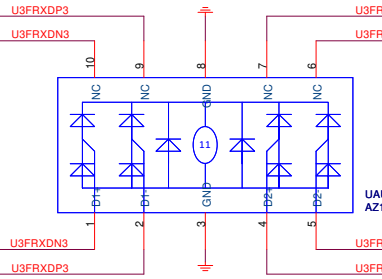
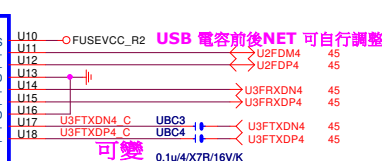
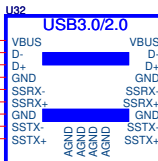
```

HUB self-power mode:
P.H.=EVERY PORT 500mA.
P.D.=EVERY PORT 100mA.

```

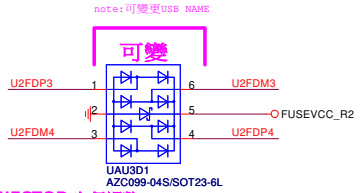
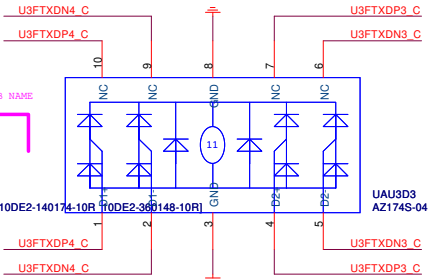


Del RAU3EC1



note:可變更USB NAME

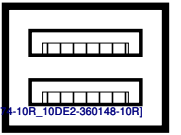
可變



CONNECTOR 自行調整

2 port USB 3.0 Capture:

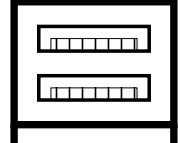
USB/18P/BU/OS/RA/D/2/1U/USB



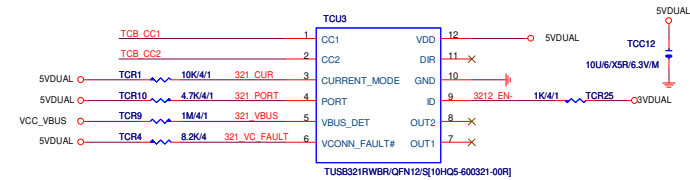
Footprint:USB30_20

2 port USB 3.0 with TYPE C Capture:

USB/18P/BU/OS/RA/D/2/HR



Footprint:USB30_H



CURRENT MODE

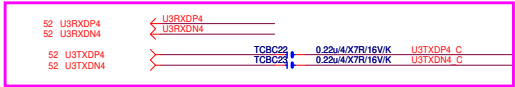
L - Default current / Pull down to GND or NC
M - Medium (1.5A) current / Pull up to VDD 500K
H - High (3.0A) current / Pull up to VDD 10K

PORT

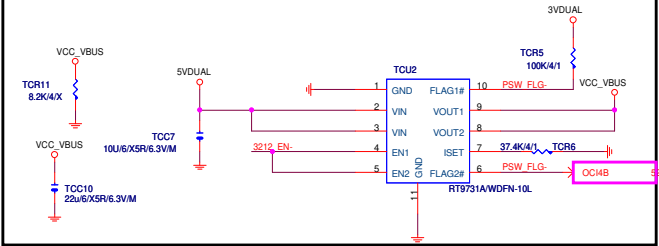
H - HOST
L - Device
NC - Dual Role

USB 3.x SuperSpeed

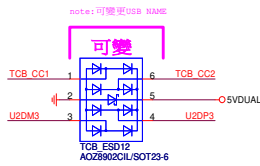
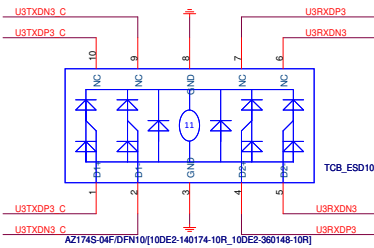
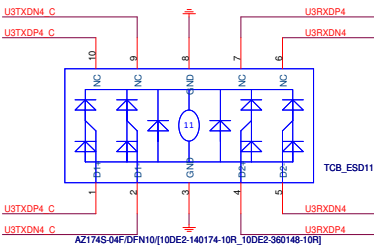
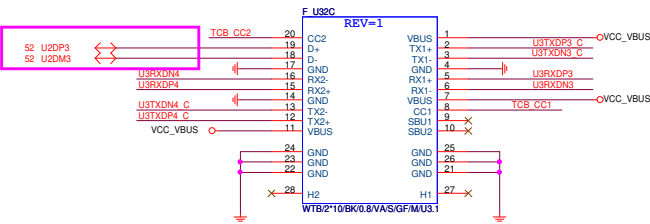
可變



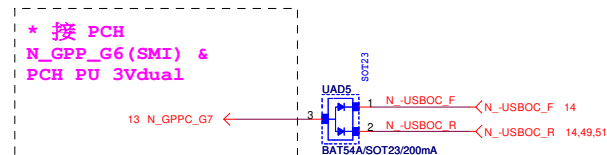
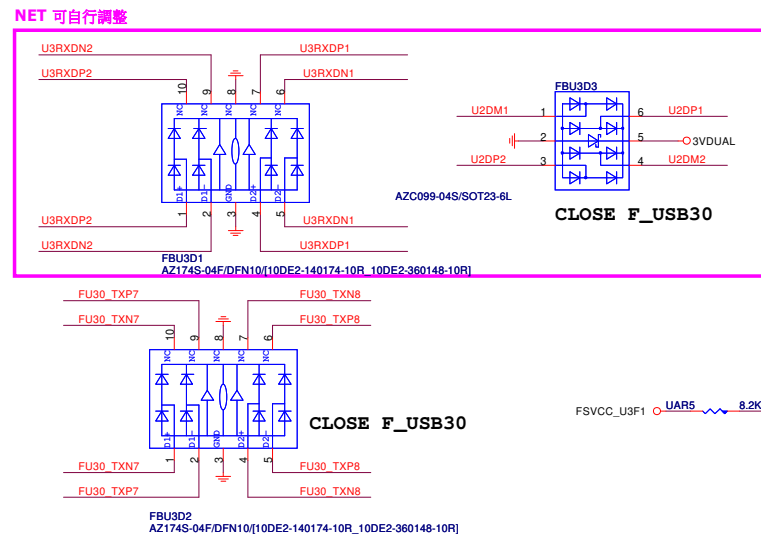
TypeC default 5V/3A



Color markers can be changed by model

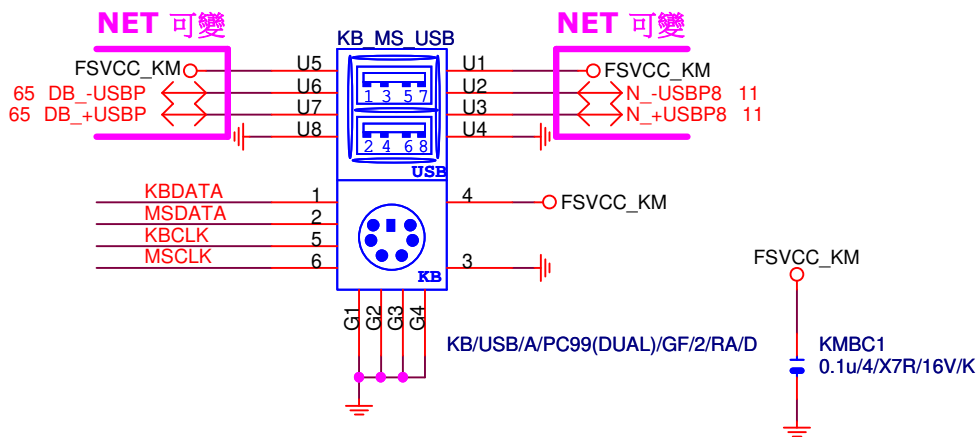


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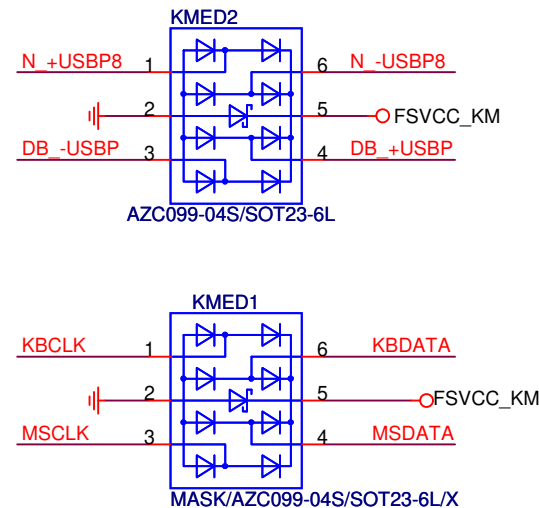


KB_MS_USB

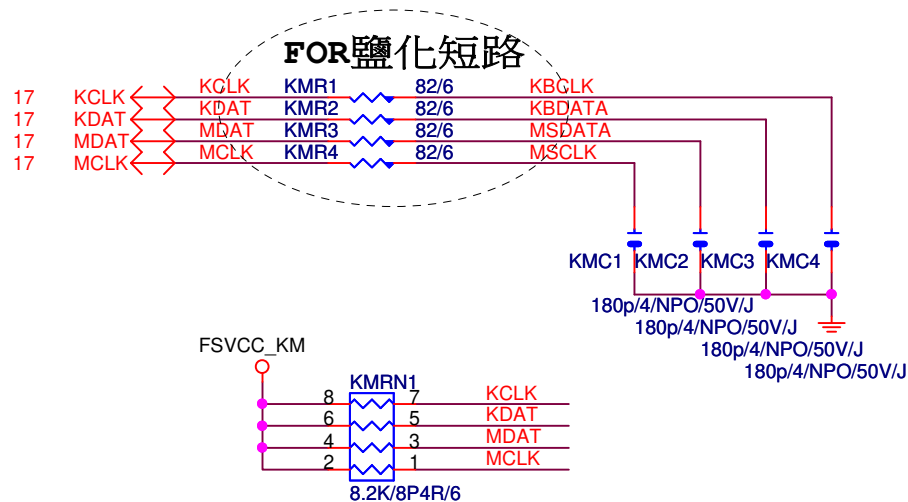
Rev: 0.7



ESD

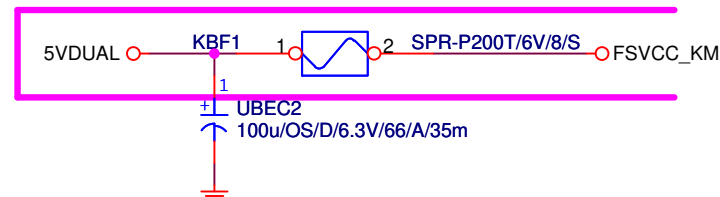


KB_MS_USB DAMPING/PU



KB_MS_USB PWR

NET 可變, 與其他USB SHARE



USB OC PROTECT

Gigabyte Technology

Title

KB_MS_USB30

Size

Document Number

Rev

B560 AORUS PRO AX

1.0

Date:

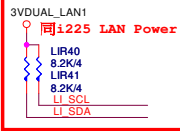
Wednesday, January 27, 2021

Sheet

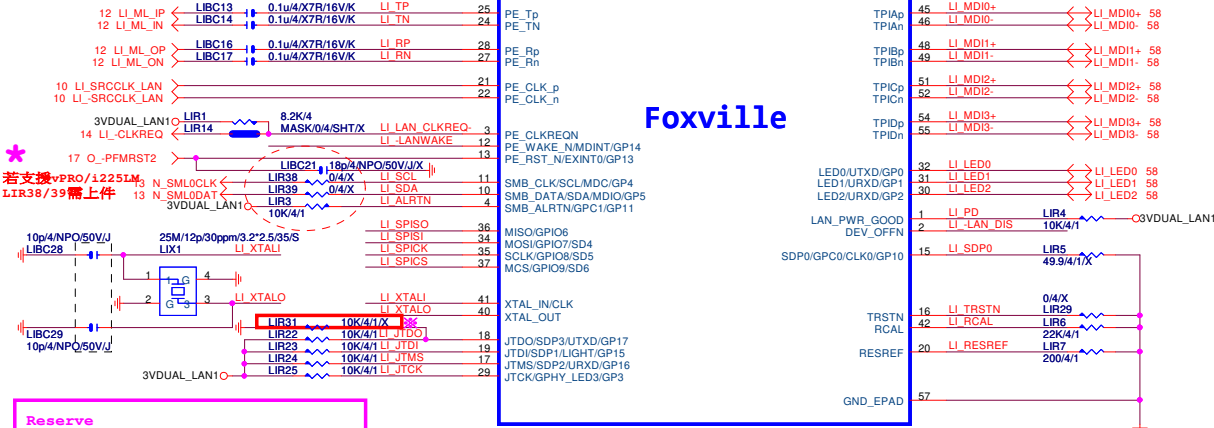
55

of

74



Lan Config	SMB (LIR38/39/21)	SMB PU (LIR40/41)
I225V + I219V	X	O
I225LM + I219LM	O	X
Only I225V	X	O
Only I225LM	O	X



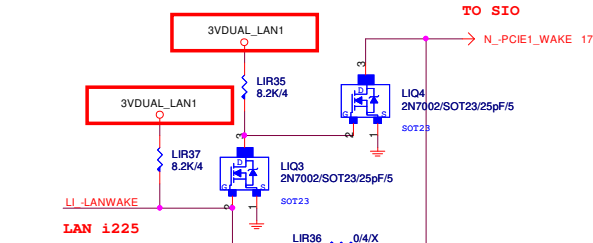
Reserve
N_SML0DAT LIR21 0.4/X LI_ALRTN

I225 monitors SMB_DATA for existing the ULP mode.

INTEL Removed MDI Lane Swap feature. (October/2019)

(組態一) PCIE LAN (Single & Dual LAN)

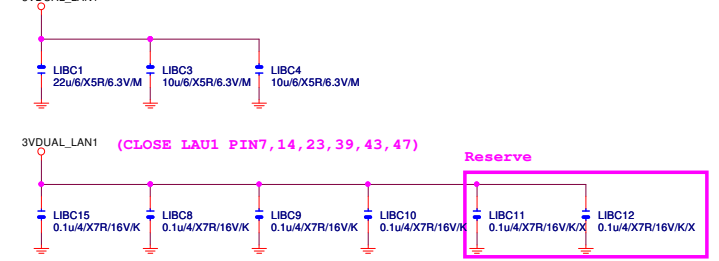
Patch LAN i225 WAKE 漏電



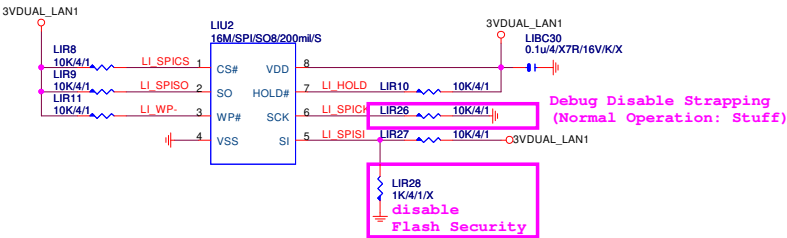
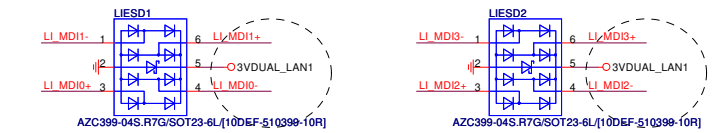
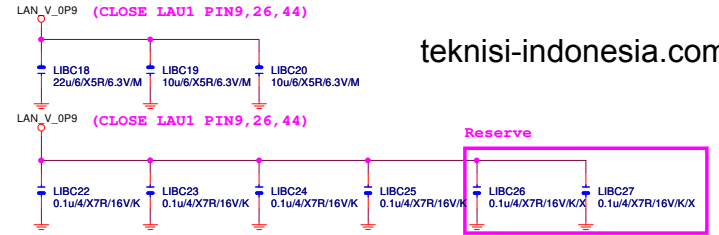
Foxville

CHIP LAN I225V B3 INTEL/[10HP2-40225V-10R]
CHIP LAN I225LM B3 INTEL/[10HP2-40225L-10R]

3VDUAL_LAN1 (CLOSE LAU1 PIN7,14,23,39,43,47) (10u X1, 2.2u X1)



(10u X1, 2.2u X2)



R1.02

note:可變更USB NAME



note:可變更USB NAME

LA MDI-->100歐姆:[20/4/8/4/20]

note:可變更USB NAME



note:可變更FUSE



note: lan power連接及電流

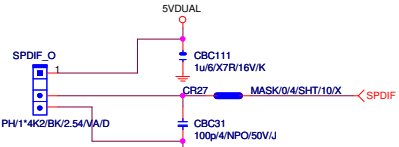
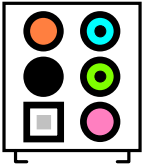


注意功耗問題！！

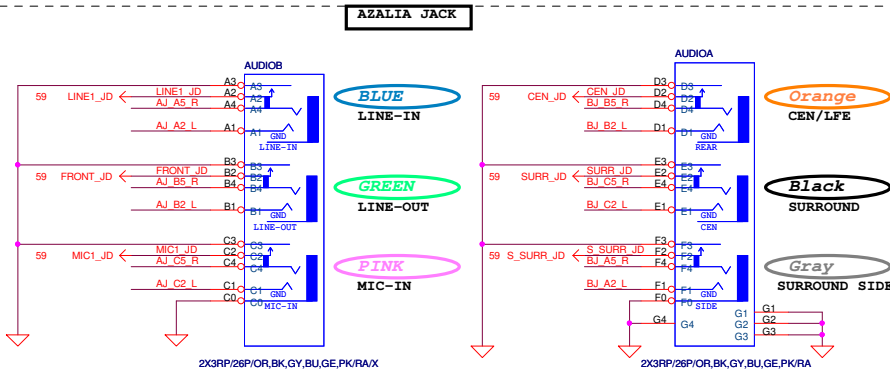
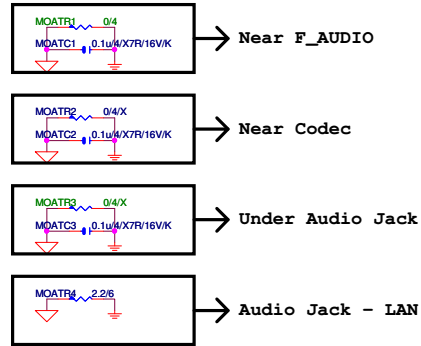
Size Custom	Document Number B560 AORUS PRO AX	Rev 1.0
Date: Wednesday, January 27, 2021	Sheet 58 of 74	

Rev 6.0

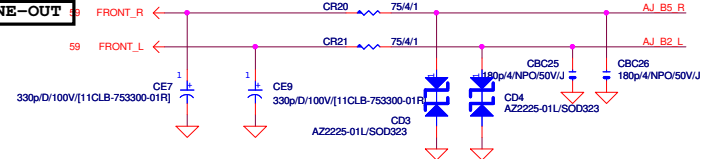
AZALIA JACK



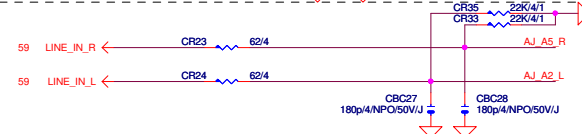
For HDMI SPDIF (依SPEC保留或移除)



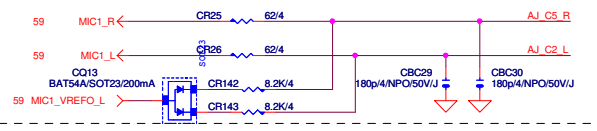
LINE-OUT



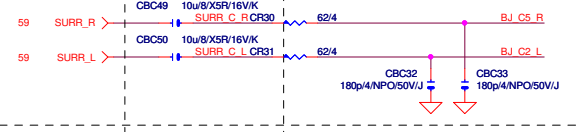
LINE-IN



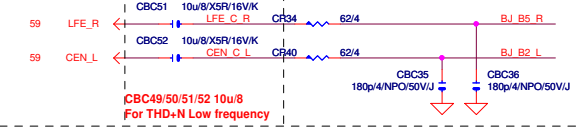
MIC-IN



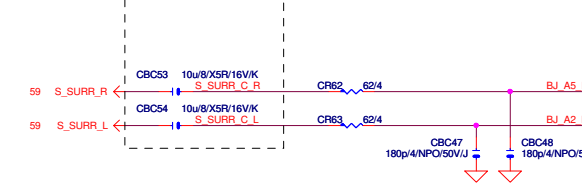
SURROUND



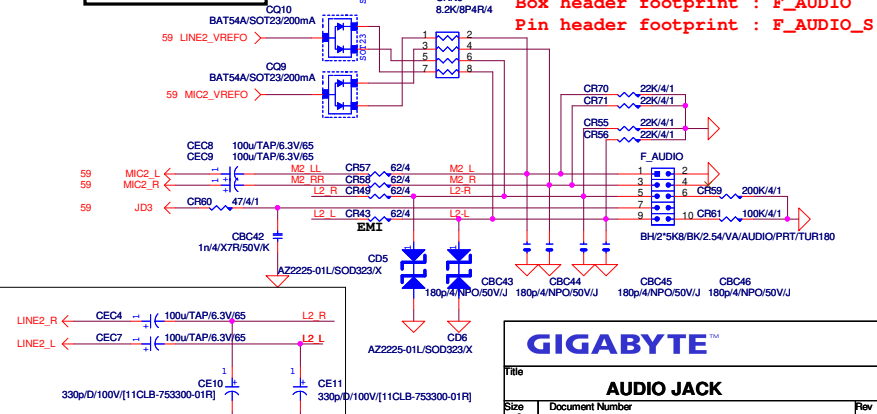
CEN/LFE



SURR BACK

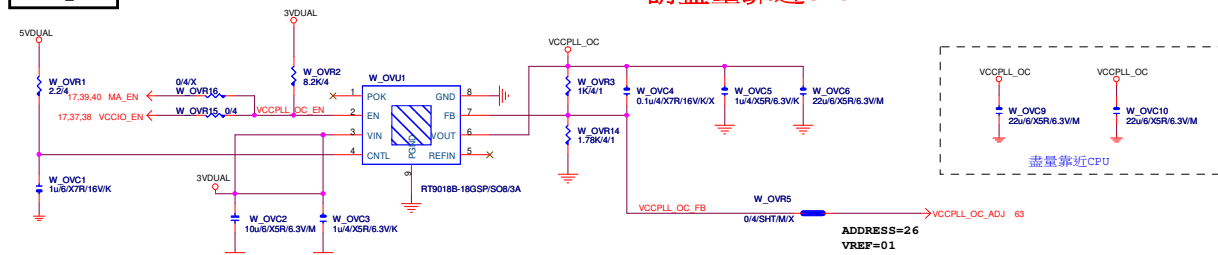


AZALIA FRONT PANEL

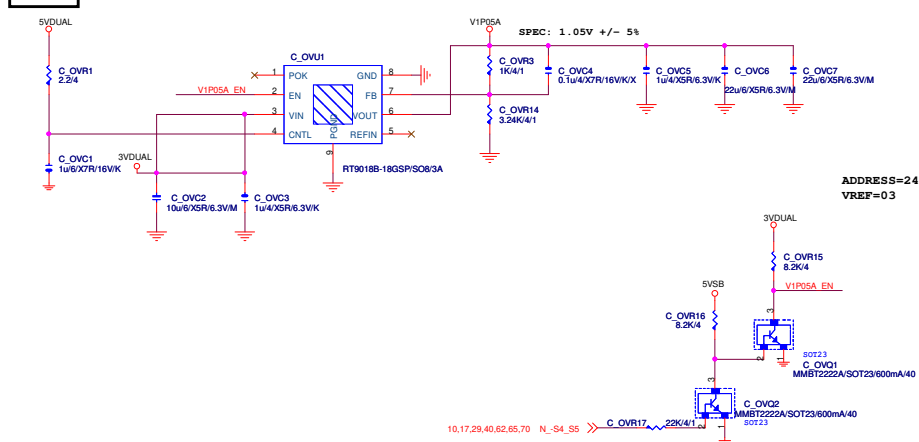


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AUDIO JACK			
B560 AORUS PRO AX			
File	Document Number	Rev	1.0
Size	Custom		
Date	Wednesday, January 27, 2021	Sheet	60 of 74

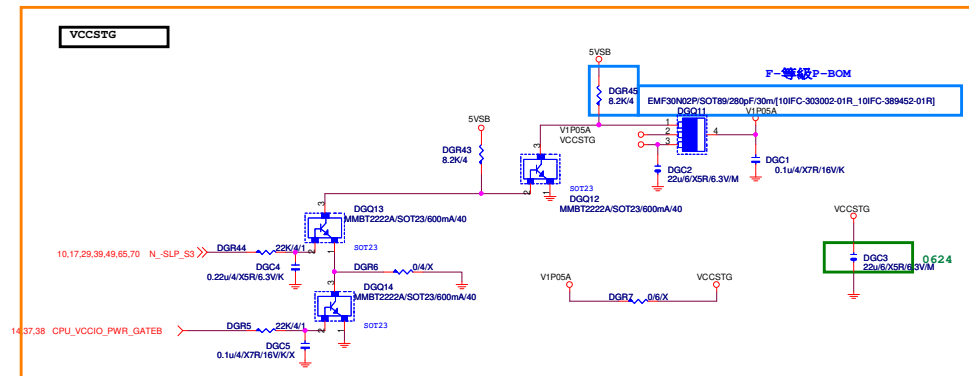
VCCPLL_OC



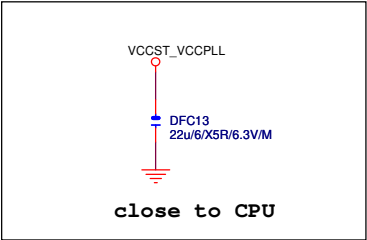
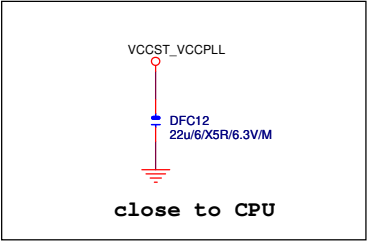
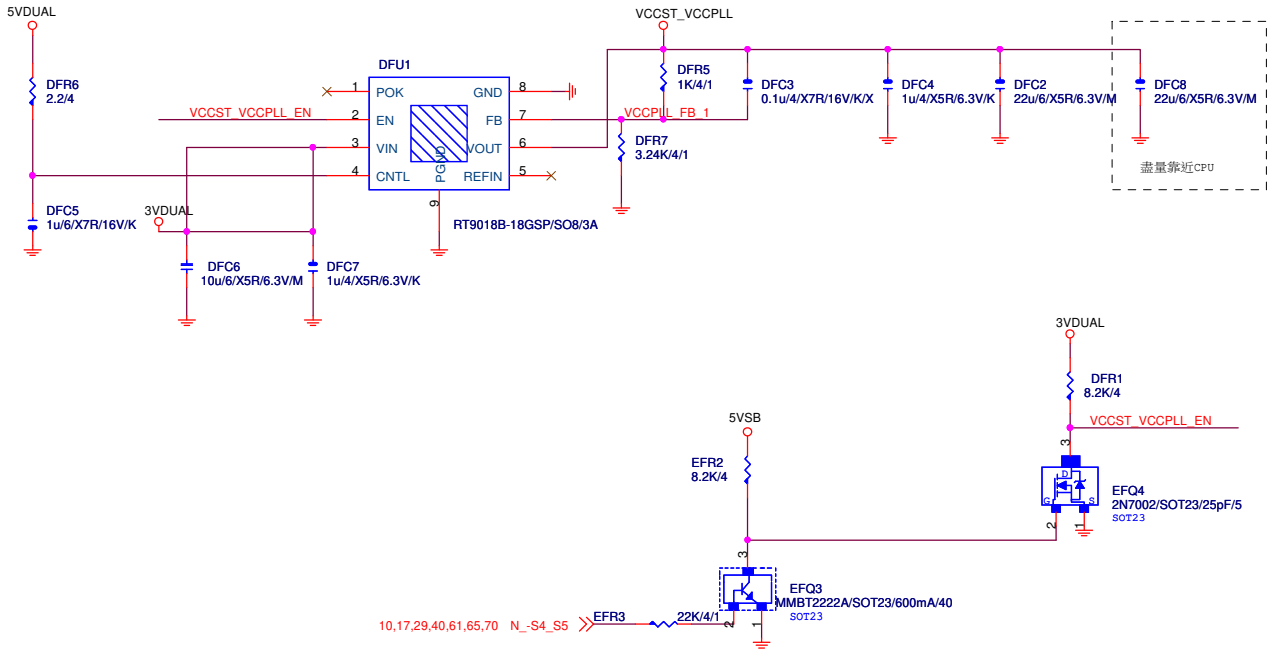
VIP05A

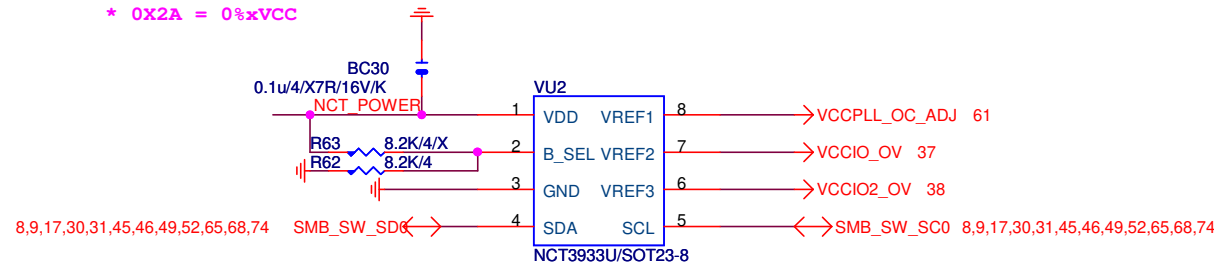
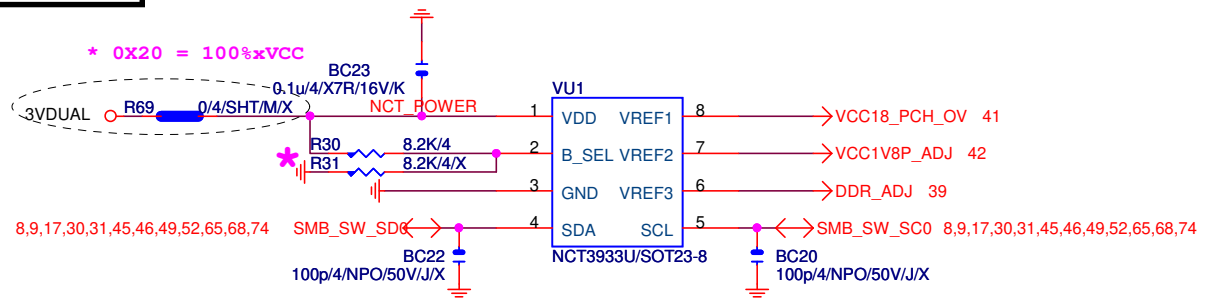

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VCCSTG



VCCST_VCCPLL 替換原先MOS開關線路





NCT3933	0X2A	0X20
VREF1	VCC18_PCH	VCCPLL_OC
VREF2	VCCIO	VCC1V8_PRIM
VREF3	VCCIO2	VDDQ

Gigabyte Technology

TitleCPU CORE VR-2

SizeCustom

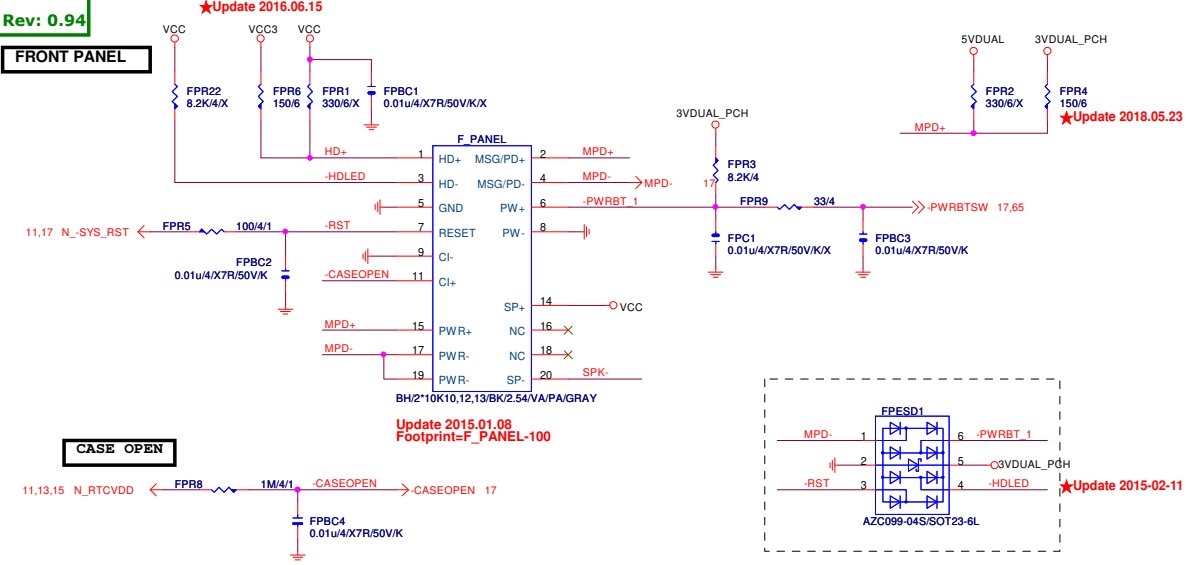
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Rev1.0

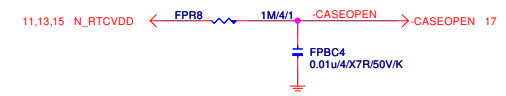
Date:Wednesday, January 27, 2021

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FRONT PANEL

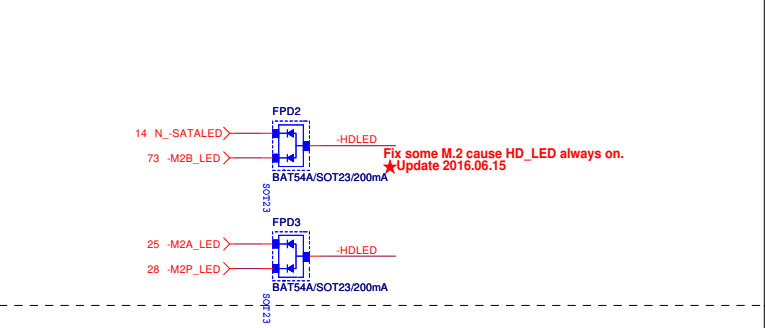


CASE OPEN

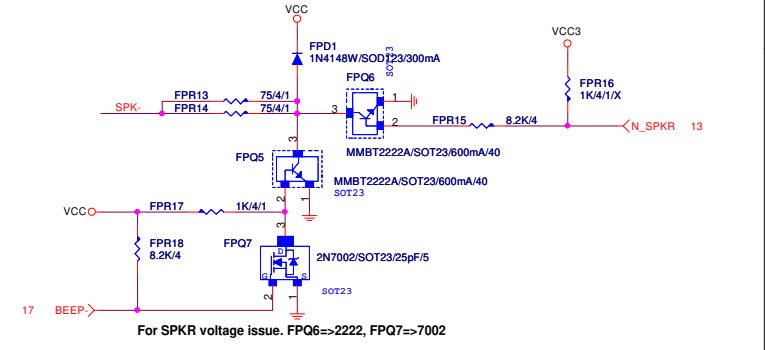


FRONT PANEL SHORT

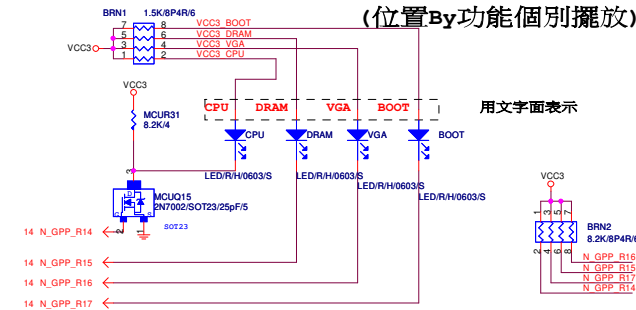
SATA/M.2 LED



SPKR W/O EC



DEBUG PORT LED *4
(位置By功能個別擺放)



N_GPP_R14	CPU DEBUG
N_GPP_R15	DDR DEBUG
N_GPP_R16	VGA DEBUG
N_GPP_R17	BOOT DEVICE DEBUG

第三區 LED

第三區 LED CONTROL

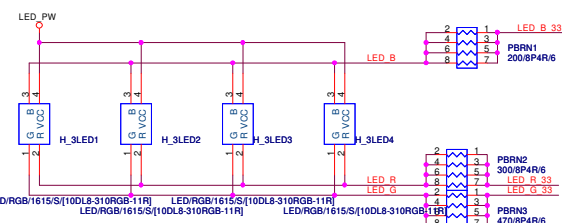
第五區 LED

第二區 LED CONTROL

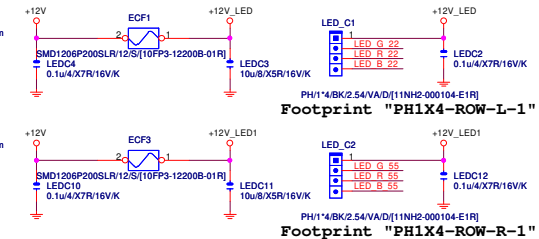
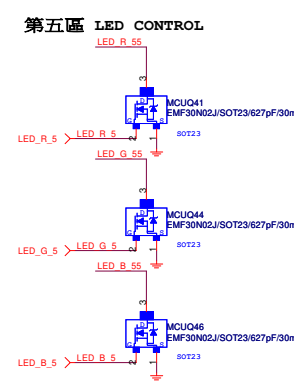
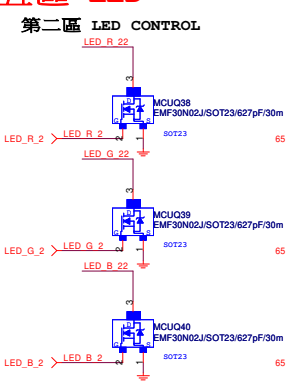
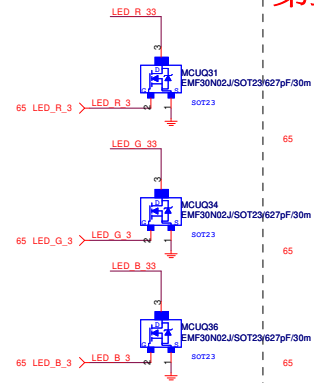
第五區 LED CONTROL

燈條 LED (LED_C1放在PCB左邊板邊位置)
燈條 LED (LED_C2放在PCB右邊板邊位置)

FOR PCH 正發光 LED*6 (位置在正板, 依據PCH_HS設計擺放)



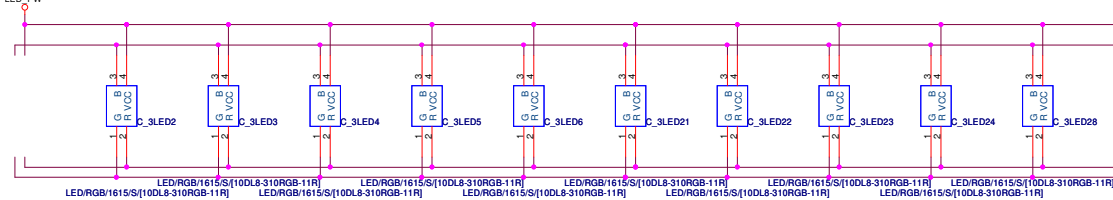
FOOTPRINT: LED-4P-RGB



第四區 LED

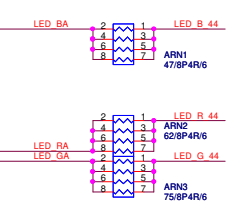
第四區 LED CONTROL

FOR AUDIO 正發光 LED*10 (位置在背板AUDIO切割線)



FOOTPRINT: LED-4P-RGB

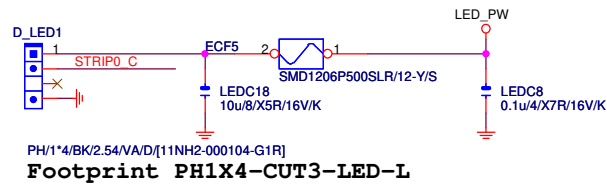
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GIGABYTE™		
PCH/AUDIO/DEBUG/C_LED1/2		
File	Document Number	Rev
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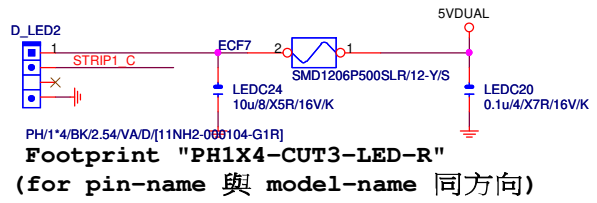
第六區 LED (靠近左上板邊位置)

Digital LED Strip1

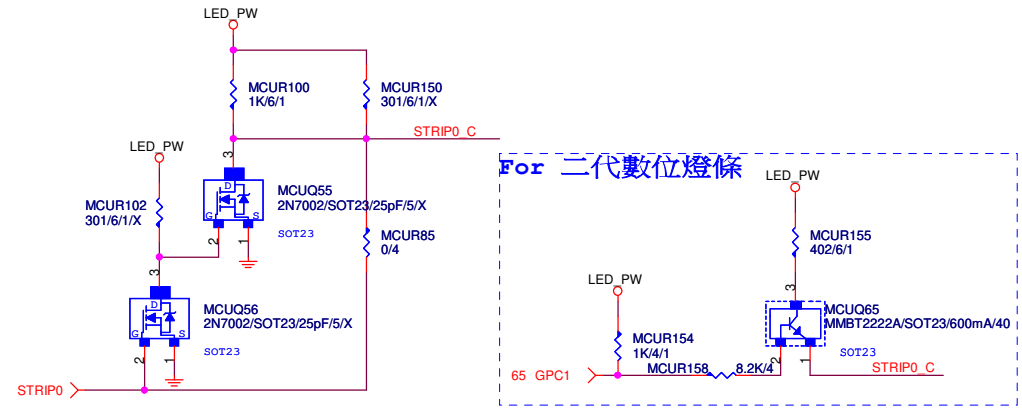


第七區 (靠近右下CPU板邊位置)

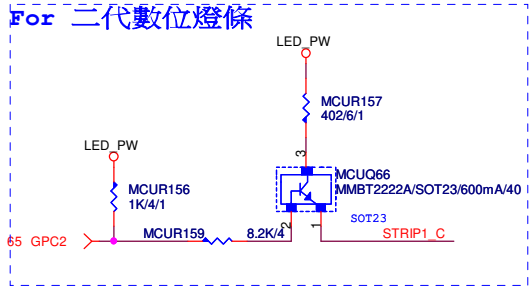
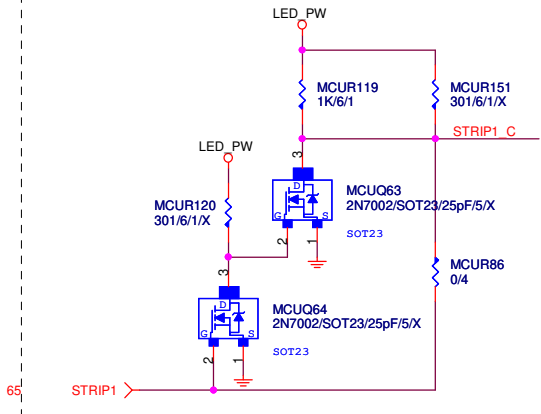
Digital LED Strip2



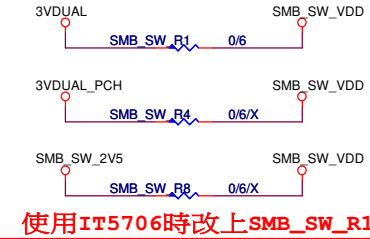
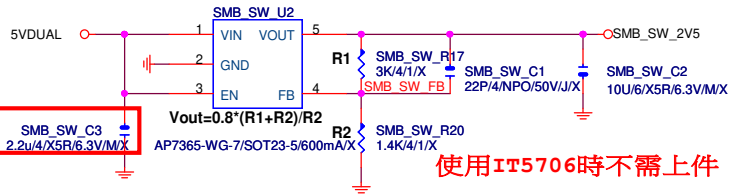
燈條 Level shift



燈條 Level shift



REV:0.1



other

8,9,17,30,31,45,46,49,52,63,65,74
8,9,17,30,31,45,46,49,52,63,65,74

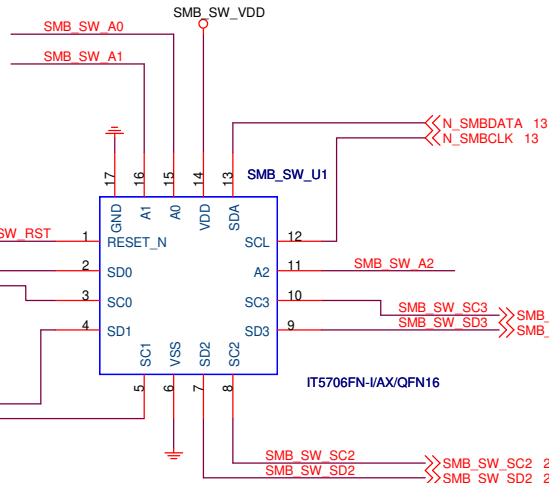
SMB_SW_SD0
SMB_SW_SC0

PCIE SLOT

21,22,23 SMB_SW_SD1
21,22,23 SMB_SW_SC1

SMB_SW_SD0
SMB_SW_SC0

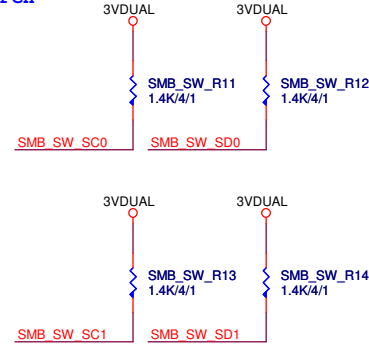
SMB_SW_SD1
SMB_SW_SC1



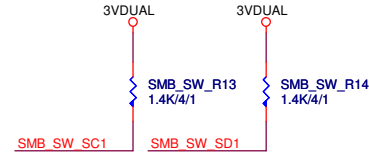
M2P_CPU使用

M2_M and M2_A

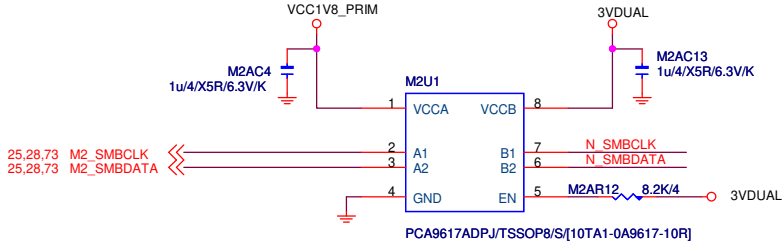
PCH



M2_B and M2_C



M2_P and M2_A



N_SMBCLK SMB_SW_R21 0/4/X SMB_SW_SC0
N_SMBDATA SMB_SW_R22 0/4/X SMB_SW_SD0
N_SMBCLK SMB_SW_R23 0/4/X SMB_SW_SC1
N_SMBDATA SMB_SW_R24 0/4/X SMB_SW_SD1

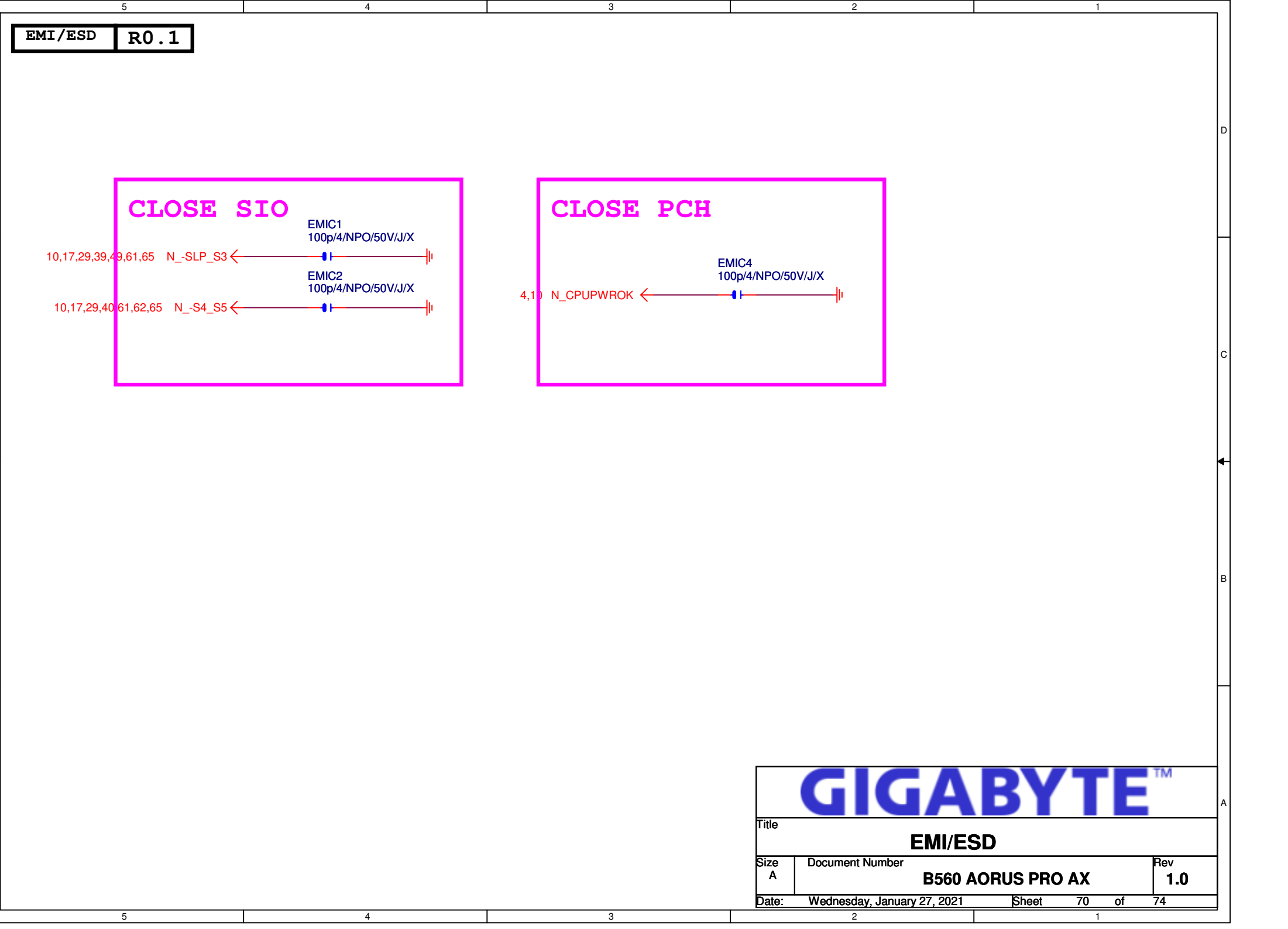
SMB_SW_U1 不上件時.電阻要上

Title

SMBUS SWITCH

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CLOSE SIO

EMIC1
100p/4/NPO/50V/J/X

10,17,29,39,49,61,65 N_-SLP_S3 ←

EMIC2
100p/4/NPO/50V/J/X

10,17,29,40 61,62,65 N_-S4_S5 ←

CLOSE PCH

EMIC4
100p/4/NPO/50V/J/X

4,1 N_CPUPWROK ←

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Title

EMI/ESD

Size
A

Document Number

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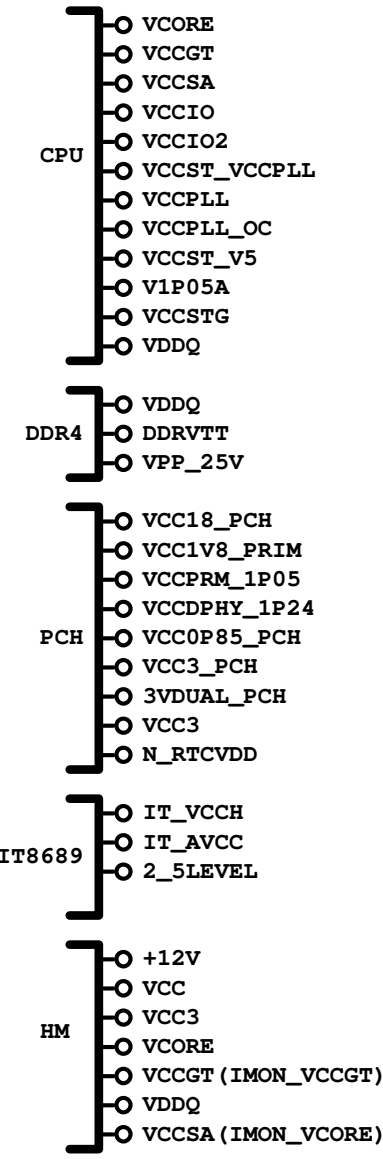
Rev

1.0

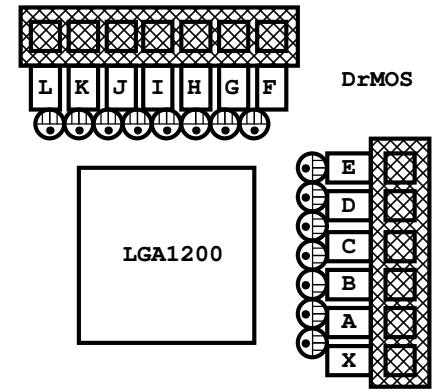
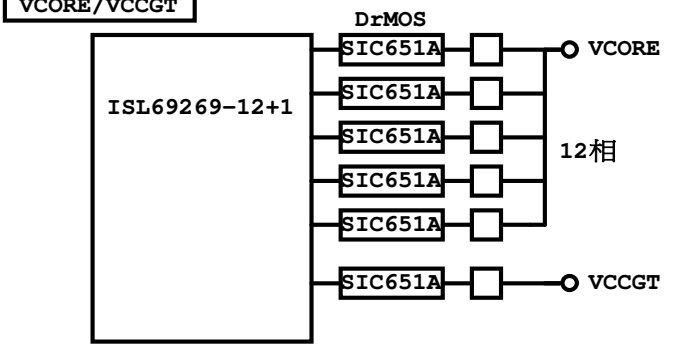
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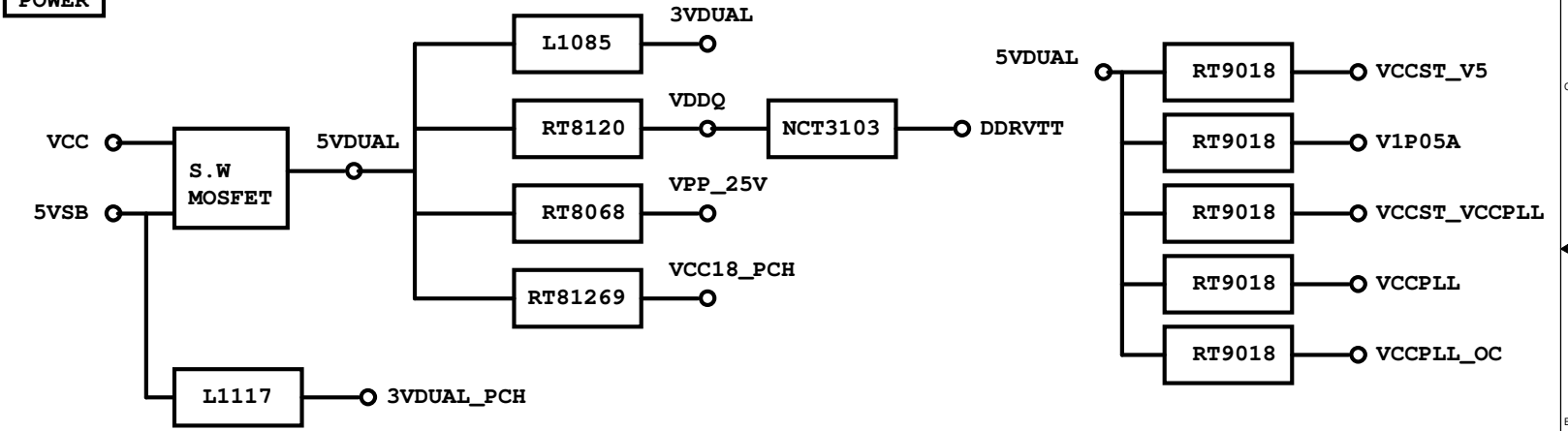
POWER BLOCK MAP



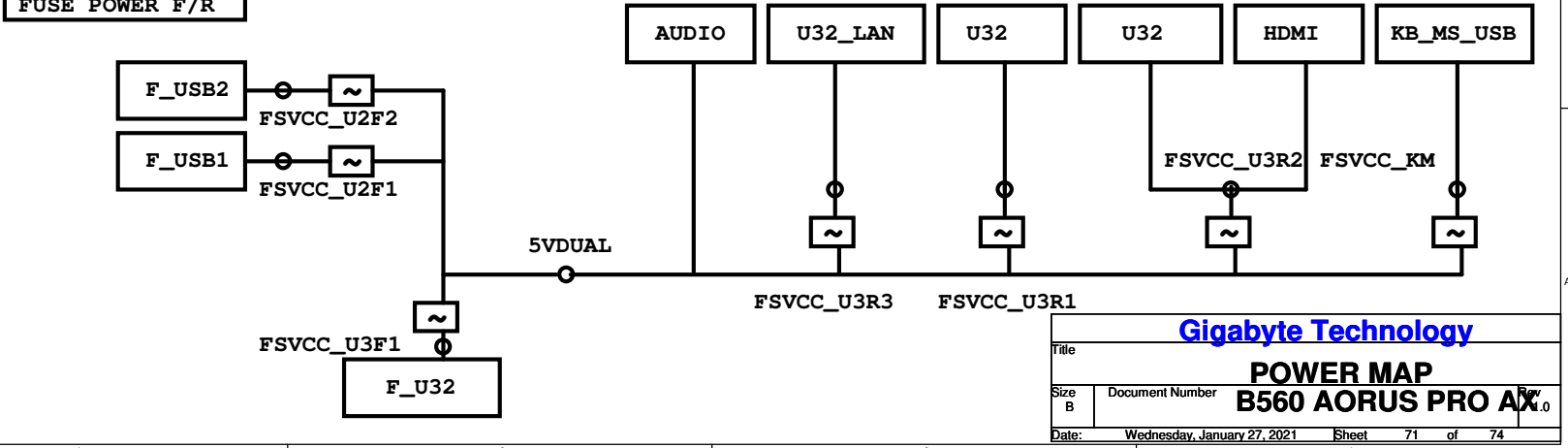
VCORE/VCCGT

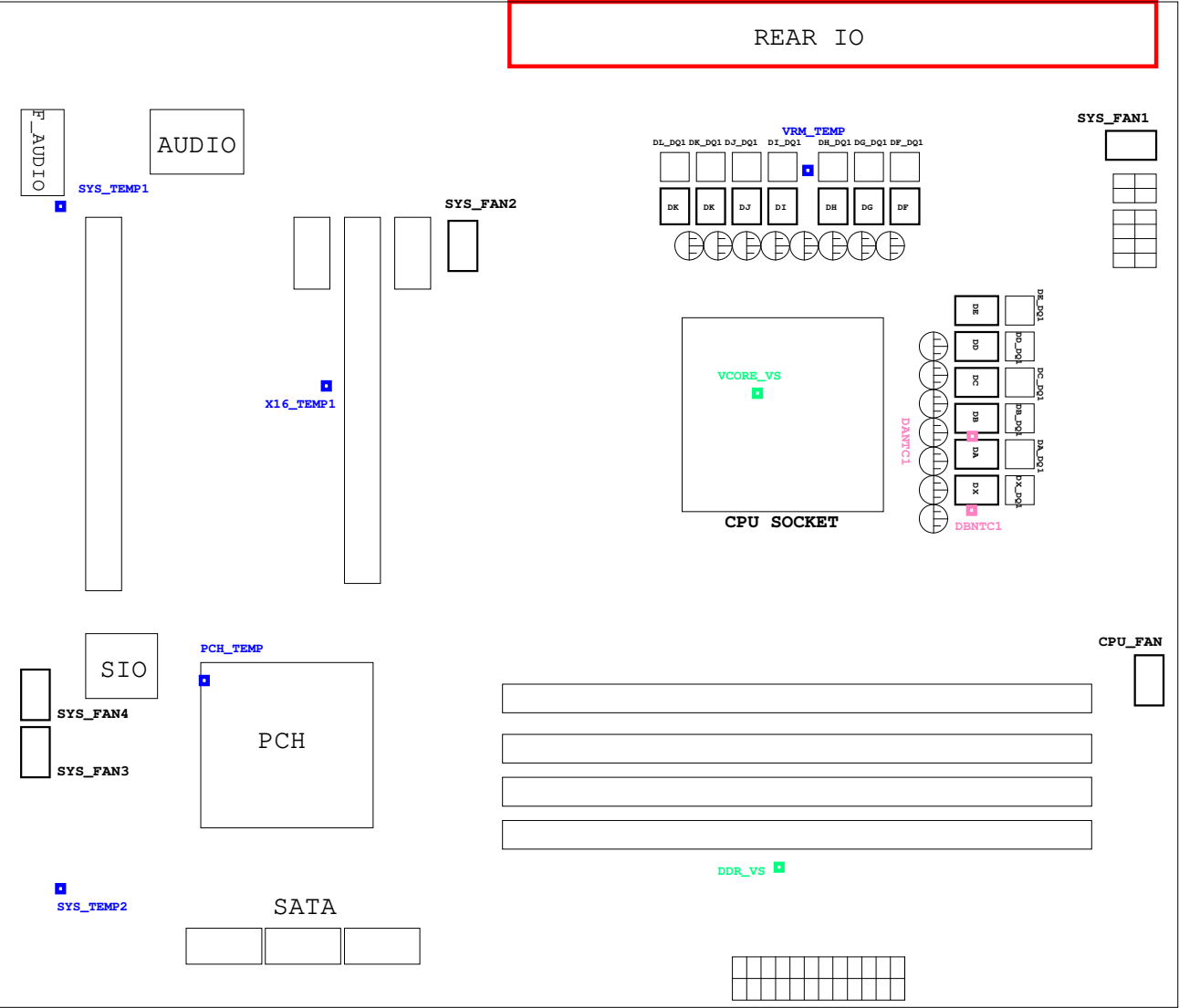


POWER



FUSE POWER F/R





熱敏電阻	擺放靠近位置	走線方式
DANTC1	DA_DL2	Differential
DANTC2	DA_DQ3	Differential
DANTC3	DM_DQ2	Differential
DANTC4	DM_DL1	Differential
VRM_TEMP	DC_DQ1	N/A
X16_TEMP1	PCIEX16	N/A
PCH_TEMP	PCH	N/A
SYS_TEMP1	F_AUDIO	N/A
SYS_TEMP2	F_PANEL	N/A

- SIO RS
- PWM RS
- SIO VIN

FAN

Rev 0.6

M.2 Lane3 from PCH port24

M.2 Lane2 from PCH port23

M.2 Lane1 from PCH port22

M.2 Lane1 from PCH port21

支援SATA and M.2 function

需與M2_-CLKREQ對應

架高 金屬加強

Footprint : m2_110_h2mm8w

SMD螺母

10KS2-040131-01R



DIP螺柱

有上M2 HEATSINK時螺柱/螺母一體式



CR{12KSF-F10303-81R}

架高

有上M2 HEATSINK時特制螺絲



CR{12KS2-110202-31R}/X

DIP螺絲

M2_SB_HS

M2 HEATSINK

M2_SB_HS{12SP1-S11705-02R_12SP1-S11705-04R_12SP1-S11705-05R}:M2_SB_HS

GIGABYTE Technology

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